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# Digital Electronics Interview Questions

INSIDE

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- Grouped by topic

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## Number systems and codes

### 1. What is 2's complement representation, and what range does it cover for n bits?

A negative number is stored as the complement of its magnitude plus one. In n bits it covers $-2^{n-1}$ to $2^{n-1}-1$, with a single zero. The same binary adder handles signed and unsigned addition, which is why hardware uses it.

### 2. What signed decimal value does the 8-bit 2's complement number 10110110 hold?

The sign bit is 1, so the value is negative. Inverting the bits and adding 1 gives the magnitude, 01001010, which is 74. The value is $-74$. As a check, 10110110 read as unsigned is 182, and $182 - 256 = -74$.

**WORKING**

1. The sign bit is 1, so the number is negative.
2. Invert the bits: 01001001.
3. Add 1: 01001010.
4. $01001010_2 = 64 + 8 + 2 = 74$, so the value is $-74$.

### 3. Why is Gray code used for shaft-position encoders instead of plain binary?

In Gray code, neighbouring values differ in exactly one bit. When the shaft moves between two adjacent positions, only one bit changes, so a misaligned read is wrong by at most one position. In binary, several bits flip together and a misread can give a wildly wrong value.

## Boolean algebra, logic gates and minimisation

### 4. Why is the NAND gate called a universal gate?

Any Boolean function can be built from NAND gates alone. Tying the inputs together gives NOT. A NAND followed by a NOT gives AND. NANDs on inverted inputs give OR, by De Morgan's law. NOR is universal for the same reason.

### 5. What is the difference between the SOP and POS forms of a Boolean function?

SOP is an OR of AND terms and is written from the rows where the output is 1 (minterms). POS is an AND of OR terms and is written from the rows where the output is 0 (maxterms). Both describe the same function and give a two-level circuit.

### 6. Why do Karnaugh map groups of 1s simplify to fewer literals, and why must a group's size be a power of 2?

Adjacent cells, including those across the map edges, differ in exactly one variable, so a group of two cancels that variable. A group can drop a variable only if it holds the cells for both of its values. So a group that drops $k$ variables holds every combination of them: $2^k$ cells. Larger groups give fewer literals.

### 7. What is a static hazard in a combinational circuit, and how is it removed in a two-level SOP circuit?

A static hazard is a brief glitch at the output when one input changes although the output should stay constant. It comes from unequal path delays. In an SOP circuit, adding the redundant consensus term that covers the transition removes it.

## Logic families and CMOS logic gates

### 8. What are the high and low noise margins of a logic gate?

The high noise margin is $NM_H = V_{OH} - V_{IH}$ and the low noise margin is $NM_L = V_{IL} - V_{OL}$. Each is the largest noise voltage a gate output can carry before the next gate misreads its level. Datasheets use worst-case values.

### 9. Why does a static CMOS gate draw almost no power when its inputs are steady?

In steady state, either the pull-up or the pull-down network is off, so there is no direct path from supply to ground. Only small leakage current flows. Most power is drawn during switching, to charge and discharge the load capacitance.

### 10. A CMOS inverter drives a 50 fF load from a 1.0 V supply. It switches at 1 GHz with an activity factor of 0.1. What is its dynamic power?

With $P = \alpha C V_{DD}^2 f$, the dynamic power is $0.1 \times 50\ \text{fF} \times (1.0\ \text{V})^2 \times 1\ \text{GHz} = 5\ \mu\text{W}$. Here $\alpha$ is the fraction of clock cycles in which the output charges the load. Short-circuit and leakage power come on top of this figure.

**WORKING**

1. Use $P = \alpha C V_{DD}^2 f$.
2. $P = 0.1 \times 50 \times 10^{-15} \times 1^2 \times 10^9$.
3. $P = 5 \times 10^{-6}$ W.

### 11. How is a 2-input CMOS NAND gate built, and how many transistors does it use?

Two NMOS transistors in series form the pull-down network. Two PMOS transistors in parallel form the pull-up network, which is the dual of the pull-down. The output is low only when both inputs are high. The gate uses four transistors.

## Combinational circuits

### 12. What is the difference between a half adder and a full adder?

A half adder adds two bits, giving sum $A \oplus B$ and carry $AB$. A full adder adds three bits, the two inputs and a carry-in, giving sum $A \oplus B \oplus C_{in}$. A full adder can be made from two half adders and an OR gate.

### 13. Why is a carry look-ahead adder faster than a ripple-carry adder?

In a ripple-carry adder each stage waits for the carry from the one before, so delay grows in proportion to the number of bits. A look-ahead adder computes all carries in parallel from generate and propagate signals, using fewer gate levels but more hardware.

### 14. How can a 4:1 multiplexer implement any function of three variables?

Connect two of the variables to the select lines. Wire each data input to 0, 1, the third variable or its complement, whichever matches the truth table for that select combination. In general a $2^k$:1 multiplexer can implement any function of $k + 1$ variables.

## Sequential circuits

### 15. What is the difference between a latch and a flip-flop?

A latch is level-sensitive: its output follows the input for as long as the enable is active. A flip-flop is edge-triggered: it samples the input only at the clock edge and holds the value until the next edge. Synchronous design relies on flip-flops.

### 16. Why does a ripple counter limit the clock speed compared with a synchronous counter?

In a ripple counter, each flip-flop is clocked by the output of the one before, so clock-to-Q delays add up across the stages. The count is also briefly wrong while the change ripples through. In a synchronous counter all flip-flops share one clock, so the delay does not accumulate.

### 17. What are setup time and hold time of a flip-flop?

Setup time is how long the data input must be stable before the active clock edge. Hold time is how long it must stay stable after the edge. If either is violated, the flip-flop may capture the wrong value or go metastable.

### 18. Two flip-flops are joined by combinational logic. The clock-to-Q delay is 0.6 ns, the logic delay is 3.4 ns and the setup time is 1.0 ns. Ignoring skew, what is the maximum clock frequency?

The clock period must cover the clock-to-Q delay, the logic delay and the setup time: $T_{min} = 0.6 + 3.4 + 1.0 = 5.0$ ns. So $f_{max} = 1/T_{min} = 200$ MHz. A faster clock would let the data reach the second flip-flop too late to meet its setup time.

**WORKING**

1. The clock period must cover $t_{clk-Q} + t_{logic} + t_{setup}$.
2. $T_{min} = 0.6 + 3.4 + 1.0 = 5.0$ ns.
3. $f_{max} = 1/T_{min} = 1/(5.0 \times 10^{-9}\ \text{s})$.
4. $f_{max} = 200$ MHz.

## Sample-and-hold, ADCs and DACs

### 19. How does a flash ADC work, and what is its drawback?

An n-bit flash ADC compares the input with $2^n - 1$ reference levels using parallel comparators, and an encoder turns the result into a code in one step. It is the fastest ADC type. The comparator count roughly doubles with every added bit, so it is used only at low resolution.

### 20. What is the difference between a successive-approximation ADC and a dual-slope ADC?

A successive-approximation ADC tests bits from the MSB down, so an n-bit conversion needs n clock cycles and is moderately fast. A dual-slope ADC integrates the input for a fixed time, then integrates a reference back down. It is slow, but it averages out noise and rejects mains interference when the fixed time is a whole number of mains periods.

### 21. An 8-bit DAC produces an output of $V_{ref} \times D/2^n$, where $D$ is the input code. With $V_{ref} = 5$ V, what is the output for code 200?

With $V_{out} = V_{ref} \times D/2^n$ and $2^8 = 256$, the output is $5 \times 200/256 = 3.90625$ V, about 3.906 V. Each code step is $5/256 \approx 19.5$ mV, and the full-scale code 255 gives about 4.98 V, not 5 V.

**WORKING**

1. Use $V_{out} = V_{ref} \times D/2^n$.
2. $2^8 = 256$.
3. $V_{out} = 5 \times 200/256$.
4. $V_{out} = 3.906$ V.

## Memories and microprocessors

### 22. What is the difference between SRAM and DRAM?

SRAM stores each bit in a cross-coupled latch, usually six transistors. It is fast and needs no refresh, but takes more area. DRAM stores a bit as charge on a capacitor with one transistor. It is denser and cheaper but needs periodic refresh. SRAM suits caches, DRAM suits main memory.

### 23. Why does pipelining raise the throughput of a processor?

Pipelining overlaps the stages of different instructions, so ideally one instruction finishes every cycle. The latency of a single instruction does not fall. Data, control and structural hazards cause stalls, so the real speed-up is below the number of stages.

### 24. How many 16K x 8 memory chips are needed to build a 64K x 16 memory?

Two chips side by side give 16-bit words ($16/8 = 2$), and four such pairs give 64K words ($64K/16K = 4$). The total is $4 \times 2 = 8$ chips. The two chips of a pair share address lines and each supplies one byte of every word.

**WORKING**

1. Chips needed to reach the word count: $64K/16K = 4$ rows.
2. Chips needed to reach the word width: $16/8 = 2$ per row.
3. Total chips: $4 \times 2 = 8$.

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