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Analog Electronics Formula Sheet

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SHOCKLEY DIODE EQUATION

$$I_D = I_S\left(e^{V_D/(nV_T)} - 1\right), \qquad V_T = \frac{kT}{q}$$

Exponential model of the junction below breakdown (series resistance neglected). I_S = reverse saturation current, n = ideality factor (1 to 2). $V_T = 25.9$ mV at 300 K; these notes round it to 25 mV, and 26 mV is also common, so take the value the question gives. For $V_D \gg nV_T$, $I_D \approx I_S e^{V_D/(nV_T)}$; for $V_D \ll -V_T$, $I_D \approx -I_S$.

FORWARD VOLTAGE CHANGE WITH CURRENT

$$V_{D2} - V_{D1} = nV_T \ln\frac{I_{D2}}{I_{D1}} = 2.303\, nV_T \log_{10}\frac{I_{D2}}{I_{D1}}$$

Valid when both currents are much larger than I_S. With $n = 1$ and $V_T = 25$ mV, a tenfold change in current changes V_D by 57.6 mV (about 60 mV with 26 mV).

DYNAMIC (SMALL-SIGNAL) RESISTANCE

$$r_d = \frac{nV_T}{I_D}$$

Slope resistance dV_D/dI_D at the dc operating current I_D (valid for $I_D \gg I_S$), used when a small ac signal rides on a dc bias. With $n = 1$, $V_T = 25$ mV and $I_D = 1$ mA, $r_d = 25\ \Omega$.

TEMPERATURE DEPENDENCE (SILICON, NEAR ROOM TEMPERATURE)

$$\frac{dV_D}{dT} \approx -2\ \text{mV/°C}\ \ (\text{constant } I_D), \qquad I_S(T_2) \approx I_S(T_1)\, 2^{(T_2 - T_1)/10}\ \ (T \text{ in } ^\circ\text{C})$$

At a fixed current the forward drop falls as temperature rises (figures between about -2 and -2.5 mV/°C are quoted, so use the value given). Problems often assume the reverse saturation current doubles for every 10 °C rise (about 7% per °C). This is a rule of thumb: some treatments give a faster rate for the ideal-junction I_S, so if a question states a rate, use it.

UPPER-LEVEL SHUNT CLIPPER

$$v_o = \min\left(v_i,\ V_R + V_\gamma\right)$$

Diode anode at the output node, cathode at potential V_R. The diode conducts, and the output is flat, for $v_i \geq V_R + V_\gamma$.

LOWER-LEVEL SHUNT CLIPPER

$$v_o = \max\left(v_i,\ V_R - V_\gamma\right)$$

Diode cathode at the output node, anode at potential V_R. The diode conducts for $v_i \leq V_R - V_\gamma$. With the anode at -5 V, for example, the output cannot fall below -5.7 V.

DOUBLE-ENDED (TWO-LEVEL) CLIPPER

$$v_o = \min\left(\max\left(v_i,\ V_2 - V_\gamma\right),\ V_1 + V_\gamma\right)$$

Two shunt branches: an upper-level diode with its cathode at potential V_1, and a lower-level diode with its anode at potential V_2, where $V_2 - V_\gamma < V_1 + V_\gamma$. The output is confined to $V_2 - V_\gamma \leq v_o \leq V_1 + V_\gamma$, and at most one diode conducts at any instant. Two identical Zener diodes connected back to back in series (anode to anode, or cathode to cathode) across the output, fed through a series resistor, clip at $\pm(V_Z + V_\gamma)$: on each half-cycle one is in breakdown and the other is forward-biased.

TOP-PINNED CLAMPER (DIODE ANODE AT OUTPUT)

$$V_{\text{shift}} = V_R + V_\gamma - V_{i,\max}, \qquad v_o = v_i + V_{\text{shift}}$$

Diode anode at the output, cathode at potential V_R. The capacitor settles at $V_C = V_{i,\max} - (V_R + V_\gamma)$, input-side plate positive. Unbiased ideal case: $v_o = v_i - V_m$, so the output runs from 0 to $-2V_m$.

BOTTOM-PINNED CLAMPER (DIODE CATHODE AT OUTPUT)

$$V_{\text{shift}} = V_R - V_\gamma - V_{i,\min}, \qquad v_o = v_i + V_{\text{shift}}$$

Diode cathode at the output, anode at potential V_R. For a sinusoid, $V_{i,\min} = -V_m$. Unbiased ideal case: $v_o = v_i + V_m$, so the output runs from 0 to $2V_m$.

CLAMPER CONDITIONS AND DC VALUE

$$R_L C \gg T, \qquad V_{o,\text{pp}} = V_{i,\text{pp}}, \qquad V_{o,\text{dc}} = V_{i,\text{dc}} + V_{\text{shift}}$$

V_{shift} is found from the actual input peaks and $V_{i,\text{dc}}$ is the input's average. For a zero-mean input such as a sinusoid, $V_{o,\text{dc}} = V_{\text{shift}}$. For a square wave, the time constant must be much larger than the interval during which the diode is OFF.

PEAK REVERSE VOLTAGE ON A CLAMPER DIODE

$$V_{D,\text{rev,max}} = |v_{o,\text{far peak}} - V_R| \qquad (= 2V_m \text{ for an unbiased ideal clamper})$$

The far peak is the output peak on the side opposite the pinned one; V_R is the signed potential of the diode's other terminal.

DEFINITIONS: DC VALUE, FORM FACTOR, RIPPLE FACTOR

$$V_{\text{dc}} = \frac{1}{T}\int_0^T v_o\,dt, \qquad \text{FF} = \frac{V_{\text{rms}}}{V_{\text{dc}}}, \qquad \text{RF} = \frac{V_{r,\text{rms}}}{V_{\text{dc}}} = \sqrt{\text{FF}^2 - 1}$$

These apply to any periodic output. $V_{r,\text{rms}} = \sqrt{V_{\text{rms}}^2 - V_{\text{dc}}^2}$ is the rms value of the ac part alone.

HALF-WAVE RECTIFIER (IDEAL DIODE, RESISTIVE LOAD)

$$V_{\text{dc}} = \frac{V_m}{\pi}, \quad V_{\text{rms}} = \frac{V_m}{2}, \quad \text{FF} = \frac{\pi}{2} = 1.57, \quad \text{RF} = 1.21$$

Currents follow the same ratios, with $I_m = V_m/R_L$. The ripple fundamental is at f, and PIV $= V_m$.

FULL-WAVE RECTIFIER (CENTRE-TAPPED OR BRIDGE, IDEAL DIODES)

$$V_{\text{dc}} = \frac{2V_m}{\pi}, \quad V_{\text{rms}} = \frac{V_m}{\sqrt{2}}, \quad \text{FF} = \frac{\pi}{2\sqrt{2}} = 1.11, \quad \text{RF} = 0.483$$

The ripple fundamental is at $2f$. PIV $= 2V_m$ for the centre-tapped circuit and V_m for the bridge.

RECTIFICATION EFFICIENCY

$$\eta = \frac{I_{\text{dc}}^2 R_L}{I_{\text{rms}}^2 (R_L + R_f)}: \qquad \eta_{\text{HW}} = \frac{4}{\pi^2}\cdot\frac{R_L}{R_L + R_f}, \qquad \eta_{\text{FW}} = \frac{8}{\pi^2}\cdot\frac{R_L}{R_L + R_f}$$

dc load power divided by the ac power fed to the rectifier. R_f is the total diode forward resistance in the conduction path: r_f for half-wave and centre-tapped, $2r_f$ for the bridge. Add winding resistance if it is given. The maxima (ideal diodes) are $4/\pi^2 = 40.5\%$ and $8/\pi^2 = 81.1\%$. The figures 40.6% and 81.2% also appear; treat them as the same result.

RECTIFIERS WITH DIODE AND WINDING RESISTANCE

$$I_m = \frac{V_m}{R_s + R_f + R_L}, \qquad V_{\text{dc}} = V_{\text{dc,NL}} - I_{\text{dc}}(R_s + R_f), \qquad \%\,\text{regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{R_s + R_f}{R_L} \times 100$$

Diodes modelled as ideal switches with forward resistance r_f (no cut-in voltage). $R_f = r_f$ for half-wave and centre-tapped, $2r_f$ for the bridge. R_s is the secondary winding resistance (one half-winding for centre-tapped). $V_{\text{dc,NL}} = V_m/\pi$ (half-wave) or $2V_m/\pi$ (full-wave), and $I_{\text{dc}} = I_m/\pi$ or $2I_m/\pi$ respectively.

TRANSFORMER UTILISATION FACTOR

$$\text{TUF} = \frac{P_{\text{dc}}}{\text{VA rating of the secondary}}$$

Ideal diodes, resistive load. Half-wave: $2\sqrt{2}/\pi^2 \approx 0.287$. Bridge: $8/\pi^2 \approx 0.81$. Centre-tapped: ≈ 0.57 for the secondary and 0.81 for the primary; the 0.69 in the table below is the average of the two. A lower TUF means a larger transformer for the same dc power. In the half-wave circuit the secondary also carries a dc current, which can saturate the core.

RECTIFIERS WITH CONSTANT-DROP DIODES

$$V_{m,\text{out}} = V_m - V_\gamma \ \ (\text{HW, CT}), \qquad V_{m,\text{out}} = V_m - 2V_\gamma \ \ (\text{bridge})$$

Use the peak output in place of V_m in the V_{dc} formula, e.g. $V_{\text{dc}} \approx (V_m - V_\gamma)/\pi$ for half-wave. This approximation slightly overestimates V_{dc}, because the diode actually conducts for less than a half-cycle. To first order in V_γ/V_m, the half-wave average is $V_m/\pi - V_\gamma/2$. PIV becomes V_m (half-wave), $2V_m - V_\gamma$ (centre-tapped) and $V_m - V_\gamma$ (bridge).

PEAK-TO-PEAK RIPPLE

$$V_r \approx \frac{V_m}{f R_L C} = \frac{I_{\text{dc}}}{fC} \ \ (\text{half-wave}), \qquad V_r \approx \frac{V_m}{2 f R_L C} = \frac{I_{\text{dc}}}{2fC} \ \ (\text{full-wave})$$

Assumes the capacitor discharges at a constant current $I_{\text{dc}} \approx V_m/R_L$ for the full period T (half-wave) or $T/2$ (full-wave), neglecting the conduction interval. This standard approximation slightly overestimates the ripple.

DC OUTPUT WITH A CAPACITOR FILTER

$$V_{\text{dc}} \approx V_m - \frac{V_r}{2}$$

Treats the ripple as a triangle between V_m and $V_m - V_r$.

RIPPLE FACTOR WITH A CAPACITOR FILTER

$$\text{RF} \approx \frac{V_r}{2\sqrt{3}\, V_{\text{dc}}} \approx \frac{1}{2\sqrt{3}\, f R_L C} \ (\text{HW}), \qquad \frac{1}{4\sqrt{3}\, f R_L C} \ (\text{FW})$$

A triangular ripple of peak-to-peak V_r has rms value $V_r/(2\sqrt{3})$. The last two forms take $V_{\text{dc}} \approx V_m$.

CONDUCTION ANGLE

$$\Delta\theta = \cos^{-1}\left(1 - \frac{V_r}{V_m}\right) \approx \sqrt{\frac{2V_r}{V_m}} \ \text{rad}$$

Angle of each charging pulse, measured from diode turn-on to the peak. Smaller ripple gives a shorter pulse and a larger peak diode current.

PIV WITH A CAPACITOR FILTER

$$\text{PIV} = 2V_m \ \ (\text{half-wave and centre-tapped}), \qquad \text{PIV} = V_m \ \ (\text{bridge})$$

Ideal diodes. Here V_m is the secondary peak (each half, for centre-tapped), which with ideal diodes equals the peak output. In the half-wave case the capacitor holds $+V_m$ on the cathode while the anode swings to $-V_m$, so the PIV is double the resistive-load value. With constant-drop diodes these become $2V_m - V_\gamma$ (half-wave and centre-tapped) and $V_m - V_\gamma$ (bridge).

VOLTAGE DOUBLER AND MULTIPLIER (NO LOAD, IDEAL DIODES)

$$V_o = 2V_m \ \ (\text{doubler}), \qquad V_o = nV_m \ \ (n\text{-stage multiplier})$$

Half-wave doubler: a clamper (C_1 charges to V_m) followed by a peak detector that captures the clamped waveform's $2V_m$ peak. Its ripple is at f, each diode sees a PIV of $2V_m$, and C_1 is rated V_m while C_2 is rated $2V_m$. Full-wave doubler: two peak detectors that charge on alternate half-cycles, stacked in series, with ripple at $2f$. Cascading more clamper–detector sections gives $3V_m$, $4V_m$ and so on. Under load the output falls below these values.

ZENER MODEL IN BREAKDOWN

$$V_Z = V_{Z0} + r_z I_Z$$

Piecewise-linear model, with r_z the Zener (dynamic) resistance. With $r_z = 0$ the output is exactly V_Z.

REGULATOR CURRENTS

$$I_R = \frac{V_S - V_Z}{R}, \qquad I_L = \frac{V_Z}{R_L}, \qquad I_Z = I_R - I_L$$

Valid only while the Zener is in breakdown.

BREAKDOWN CONDITION

$$\frac{V_S R_L}{R + R_L} \geq V_Z$$

If this fails, the Zener is OFF and $V_o = V_S R_L/(R + R_L)$.

LOAD LIMITS FOR FIXED V_S AND R

$$I_{L,\max} = I_R - I_{Z,\min}, \qquad R_{L,\min} = \frac{V_Z}{I_R - I_{Z,\min}} \left(= \frac{V_Z R}{V_S - V_Z} \text{ if } I_{Z,\min} = 0 \right)$$

A heavier load (smaller R_L) takes current away from the Zener, and below $R_{L,\min}$ the Zener drops out of breakdown. At the other end, $I_{L,\min} = I_R - I_{Z,\max}$. If that is zero or negative, running with no load is safe.

SERIES-RESISTOR DESIGN RANGE

$$\frac{V_{S,\max} - V_Z}{I_{Z,\max} + I_{L,\min}} \leq R \leq \frac{V_{S,\min} - V_Z}{I_{Z,\min} + I_{L,\max}}$$

Upper limit: at minimum input and maximum load, the Zener must still get $I_{Z,\min}$. Lower limit: at maximum input and minimum load, the Zener must not exceed $I_{Z,\max}$. If the lower limit comes out above the upper one, no value of R meets the specification.

WORST-CASE ZENER DISSIPATION

$$P_{Z,\max} = V_Z \left(\frac{V_{S,\max} - V_Z}{R} - I_{L,\min} \right)$$

Occurs at maximum input with minimum load (usually no load, $I_{L,\min} = 0$).

LINE REGULATION, OUTPUT RESISTANCE AND LOAD REGULATION

$$\frac{\Delta V_o}{\Delta V_S} = \frac{r_z \parallel R_L}{R + r_z \parallel R_L}, \qquad R_o = R \parallel r_z, \qquad \text{Load reg.} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

Small-change results from the $V_{Z0} + r_z I_Z$ model. A change in load current shifts the output by $\Delta V_o = -R_o \, \Delta I_L$. Line regulation is also quoted as a percentage or in mV/V. With $r_z = 0$ both regulations are perfect.

LED EMISSION WAVELENGTH

$$\lambda = \frac{hc}{E_g} \quad \Rightarrow \quad \lambda\,(\mu\text{m}) \approx \frac{1.24}{E_g\,(\text{eV})}$$

Photon energy is approximately the bandgap. For example, $E_g = 1.42$ eV gives $\lambda \approx 0.87$ μm (infrared). The same relation gives the longest wavelength a photodiode with bandgap E_g can detect.

VARACTOR JUNCTION CAPACITANCE AND TUNED FREQUENCY

$$C_j = \frac{C_{j0}}{(1 + V_R/V_{bi})^m}, \qquad f_0 = \frac{1}{2\pi\sqrt{LC_j}}$$

V_R = reverse bias, V_{bi} = built-in potential. $m = 1/2$ for an abrupt junction and $1/3$ for a linearly graded one; hyperabrupt junctions have $m > 1/2$. Raising V_R lowers C_j and raises the tuned frequency (when C_j is the only tuning capacitance).

BJT and MOSFET biasing and DC analysis

TERMINAL CURRENTS IN THE ACTIVE REGION

$$I_C = \beta I_B, \qquad I_E = I_B + I_C = (\beta + 1) I_B, \qquad \alpha = \frac{\beta}{\beta + 1}, \quad I_C = \alpha I_E$$

Forward-active region only. With leakage included, $I_C = \beta I_B + (\beta + 1) I_{CO}$. That is the form used to define the stability factor S.

EXPONENTIAL MODEL OF THE ACTIVE REGION

$$I_C = I_S \, e^{V_{BE}/V_T}, \qquad V_{BE2} - V_{BE1} = V_T \ln \frac{I_{C2}}{I_{C1}}$$

Forward active with $V_{BE} \gg V_T$ and the Early effect neglected. I_S is the saturation current, proportional to the emitter area, and V_T is the thermal voltage (25 mV or 26 mV at room temperature; use the question's value). The constant-drop model replaces this curve by a fixed V_{BE}. Each decade of collector current changes V_{BE} by $V_T \ln 10$: about 58 mV with $V_T = 25$ mV, or 60 mV with $V_T = 26$ mV. If an Early voltage V_A is given, multiply I_C by $(1 + V_{CE}/V_A)$; the output resistance is then $r_o = V_A / I_C$.

DC LOAD LINE

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C (R_C + R_E)$$

KVL round the collector loop, drawn on the I_C–V_{CE} output characteristics, for circuits in which R_C carries I_C (in collector-feedback bias it carries I_E; see the next section). The intercepts are $V_{CE} = V_{CC}$ at $I_C = 0$ (the cut-off end) and $I_C = V_{CC}/(R_C + R_E)$ at $V_{CE} = 0$. The approximate form takes $I_E \approx I_C$ (large β).

COLLECTOR CURRENT AT SATURATION

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C + R_E}$$

The largest collector current the external circuit allows, however hard the base is driven. With $R_E = 0$ it is exact: $(V_{CC} - V_{CE(sat)})/R_C$. With R_E present it assumes $I_E \approx I_C$, which can be poor in saturation because the base current is no longer small compared with I_C and also flows in R_E; for an exact answer solve the base and collector loops together.

Q-POINT FOR MAXIMUM SYMMETRICAL SWING (AC LOAD LINE)

$$I_{CQ} = \frac{V_{CC}}{R_{dc} + R_{ac}}, \qquad V_{CEQ} = I_{CQ} R_{ac}$$

Use this when the signal-frequency load differs from the DC load. $R_{dc} = R_C + R_E$ is the DC collector-loop resistance. R_{ac} is what the collector sees at signal frequencies, e.g. $R_C \parallel R_L$ with R_E bypassed. It places the Q-point at the middle of the AC load line, and neglects $V_{CE(sat)}$ and leakage and takes $I_E \approx I_C$. With $R_{ac} = R_{dc}$ it reduces to the midpoint, $V_{CEQ} = V_{CC}/2$.

MASTER BASE-LOOP EQUATION (ACTIVE REGION)

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta + 1) R_x}, \qquad I_C = \frac{\beta \, (V_{BB} - V_{BE})}{R_{BB} + (\beta + 1) R_x}$$

npn, forward active, leakage neglected. Read V_{BB}, R_{BB} and R_x for each circuit from the table below, then find V_{CE} from the collector loop and check that it exceeds $V_{CE(sat)}$.

FIXED BIAS

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}, \qquad I_C = \beta I_B, \qquad V_{CE} = V_{CC} - I_C R_C$$

I_B is fixed by R_B alone, so I_C is directly proportional to β. Changing the transistor, or its temperature, changes I_{CQ} by the same fraction as β changes.

COLLECTOR-TO-BASE (COLLECTOR-FEEDBACK) BIAS

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}, \qquad V_{CE} = V_{CC} - I_E(R_C + R_E)$$

R_B runs from collector to base. R_C carries $I_C + I_B = I_E$, not I_C. Put $R_E = 0$ if there is no emitter resistor. If I_C tries to rise, V_C falls and so does I_B: that is the negative feedback.

VOLTAGE-DIVIDER BIAS: EXACT (THÉVENIN) ANALYSIS

$$V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2}, \qquad R_{BB} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}, \qquad I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta + 1)R_E}$$

Exact within the constant-drop model. Use it whenever β is given and the approximate condition below is not clearly met, or when the question asks how I_C changes with β.

VOLTAGE-DIVIDER BIAS: APPROXIMATE ANALYSIS

$$V_B \approx V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2}, \qquad I_C \approx I_E = \frac{V_{BB} - V_{BE}}{R_E}, \qquad \text{valid if } \beta R_E \geq 10 R_2$$

Ignores the base current's loading of the divider. Under the stated condition, $R_{BB}/((\beta + 1)R_E) < 0.1$, so I_E is overestimated by less than 10% (and I_C by a further factor $(\beta + 1)/\beta$). The larger $\beta R_E / R_2$, the smaller the error. The result does not depend on β, which is why this circuit gives a Q-point that is nearly independent of the transistor's β.

DEFINITIONS OF THE STABILITY FACTORS

$$S = \frac{\partial I_C}{\partial I_{CO}}, \qquad S' = \frac{\partial I_C}{\partial V_{BE}}, \qquad S'' = \frac{\partial I_C}{\partial \beta}$$

Each partial derivative holds the other two parameters constant. S has no units, S' is in A/V and negative (I_C falls as V_{BE} rises), and S'' is in A.

TOTAL DRIFT OF THE COLLECTOR CURRENT

$$\Delta I_C \approx S\,\Delta I_{CO} + S'\,\Delta V_{BE} + S''\,\Delta\beta$$

First-order, for small changes. When temperature rises, $\Delta V_{BE} < 0$ and $S' < 0$, so the V_{BE} term also increases I_C. All three terms push I_C the same way.

GENERAL EXPRESSION FOR S

$$S = \frac{1 + \beta}{1 - \beta \dfrac{\partial I_B}{\partial I_C}}$$

Obtained by differentiating $I_C = \beta I_B + (1 + \beta) I_{CO}$ with respect to I_C at constant β. Get $\partial I_B / \partial I_C$ from the circuit's base-loop KVL. It is zero for fixed bias and negative whenever the circuit has feedback, which is what pulls S below $1 + \beta$.

S FOR ANY CIRCUIT OF THE MASTER FORM

$$S = \frac{(1 + \beta)(R_{BB} + R_x)}{R_{BB} + (1 + \beta)R_x} = \frac{1 + \beta}{1 + \dfrac{\beta R_x}{R_{BB} + R_x}}$$

R_{BB} and R_x come from the bias-circuit table. S runs from $1 + \beta$ for fixed bias ($R_x = 0$) down to about $1 + R_{BB}/R_x$ when $(1 + \beta)R_x \gg R_{BB}$. A small R_{BB}/R_E ratio therefore means good stability.

S′ (SENSITIVITY TO V_BE)

$$S' = \frac{-\beta}{R_{BB} + (1 + \beta)R_x}$$

Master form. Fixed bias: $S' = -\beta / R_B$. Divider or emitter bias: $S' \approx -1/R_E$ when $(1 + \beta)R_E \gg R_{BB}$ and $\beta \gg 1$.

S″ (SENSITIVITY TO B), SMALL CHANGE

$$S'' = \frac{I_C\, S}{\beta\,(1+\beta)}$$

Master form, leakage neglected. For fixed bias ($S = 1+\beta$), $S'' = I_C/\beta = I_B$, the largest possible for a given I_C and β.

S″ FOR A LARGE CHANGE OF B

$$S'' = \frac{\Delta I_C}{\Delta\beta} = \frac{I_{C1}\, S_2}{\beta_1\,(1+\beta_2)}$$

Exact within the master form (leakage neglected) when β changes from β_1 to β_2. I_{C1} is the collector current at β_1, and S_2 is S evaluated with β_2. Then $\Delta I_C = S''\,(\beta_2 - \beta_1)$.

CONDITION FOR SATURATION

$$I_B > I_{B(EOS)} = \frac{I_{C(sat)}}{\beta}, \qquad I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$I_{B(EOS)}$ is the base current at the edge of saturation. Emitter grounded; with an emitter resistor, use $R_C + R_E$ and solve both loops together. To guarantee saturation for every device of a type, use β_{min}.

FORCED BETA AND OVERDRIVE FACTOR

$$\beta_{\text{forced}} = \frac{I_{C(sat)}}{I_B} < \beta, \qquad \text{ODF} = \frac{I_B}{I_{B(EOS)}} = \frac{\beta}{\beta_{\text{forced}}}$$

In saturation, the ratio I_C/I_B is set by the external circuit, not by the transistor. The transistor is saturated when $\beta_{\text{forced}} < \beta$ (ODF > 1). Designs deliberately keep β_{forced} well below β for a margin.

TRIODE (LINEAR, OHMIC) REGION

$$I_D = k_n\left[(V_{GS} - V_{TH})\,V_{DS} - \frac{V_{DS}^2}{2}\right], \qquad V_{GS} \geq V_{TH}, \quad 0 \leq V_{DS} \leq V_{GS} - V_{TH}$$

The channel exists all the way from source to drain. The current depends on both V_{GS} and V_{DS}.

SATURATION REGION

$$I_D = \frac{1}{2}k_n(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}), \qquad V_{GS} \geq V_{TH}, \quad V_{DS} \geq V_{GS} - V_{TH}$$

The channel is pinched off at the drain end. With $\lambda = 0$, I_D does not depend on V_{DS}, and the triode and saturation equations agree at the boundary $V_{DS} = V_{OV}$, where $I_D = \frac{1}{2}k_n V_{DS}^2$. When λ is given, the small-signal output resistance is $r_o \approx 1/(\lambda I_D)$.

SATURATION TEST FROM TERMINAL VOLTAGES

$$\text{saturation} \iff V_{GD} \leq V_{TH} \iff V_D \geq V_G - V_{TH}$$

Equivalent to $V_{DS} \geq V_{OV}$ (NMOS, device on). Handy when node voltages are known: the drain may sit at most V_{TH} below the gate. If $V_{GD} > V_{TH}$, a channel exists at the drain end as well and the device is in triode.

DEEP-TRIODE ON RESISTANCE

$$r_{DS} = \frac{1}{k_n(V_{GS} - V_{TH})}, \qquad V_{DS} \ll 2(V_{GS} - V_{TH})$$

The V_{DS}^2 term is negligible here, so the MOSFET behaves as a resistor controlled by V_{GS}. This is the ON resistance of a MOSFET switch.

DEPLETION NMOS

$$I_{DSS} = \frac{1}{2}k_n V_{TH}^2, \qquad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{TH}}\right)^2 \quad \text{(saturation)}$$

For a depletion NMOS, $V_{TH} < 0$ (often written V_P). A channel already exists at $V_{GS} = 0$, and I_{DSS} is the saturation current there. The same triode and saturation equations and tests apply. V_{GS} may be negative (depletion mode) or positive (enhancement mode).

ENHANCEMENT PMOS

$$I_{SD} = \frac{1}{2}k_p(V_{SG} - |V_{TP}|)^2, \qquad \text{on if } V_{SG} \geq |V_{TP}|, \quad \text{saturated if } V_{SD} \geq V_{SG} - |V_{TP}|$$

Here $V_{TP} < 0$ and $k_p = \mu_p C_{ox}(W/L)$. Current flows from source to drain. In triode ($V_{SD} < V_{SG} - |V_{TP}|$), $I_{SD} = k_p[(V_{SG} - |V_{TP}|)V_{SD} - V_{SD}^2/2]$. Working with V_{SG}, V_{SD} and $|V_{TP}|$ keeps every quantity positive, and the NMOS rules carry over unchanged.

BODY EFFECT

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

NMOS whose source is above its body ($V_{SB} \geq 0$). V_{TH0} is the threshold at $V_{SB} = 0$, γ is the body-effect coefficient (in $V^{1/2}$) and ϕ_F is the substrate's Fermi potential; use the symbols the question gives. The threshold rises as V_{SB} rises, which lowers I_D at a given V_{GS}.

BIAS LINE AND THE ROOT THAT KEEPS THE DEVICE ON

$$V_{GS} = V_X - I_D R_X, \qquad V_{OV} = \frac{-1 + \sqrt{1 + 2k_n R_X(V_X - V_{TH})}}{k_n R_X}, \qquad I_D = \frac{1}{2}k_n V_{OV}^2$$

This is the positive root of $\frac{1}{2}k_n R_X V_{OV}^2 + V_{OV} - (V_X - V_{TH}) = 0$, assuming saturation, $\lambda = 0$ and $R_X > 0$. It needs $V_X > V_{TH}$; otherwise the device is off. Afterwards, check $V_{DS} \geq V_{OV}$. With $R_X = 0$, simply $V_{OV} = V_X - V_{TH}$.

DIODE-CONNECTED MOSFET

$$V_{DS} = V_{GS} \;\Rightarrow\; \text{saturation whenever } V_{GS} > V_{TH}, \qquad V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{k_n}}$$

Gate tied to drain (enhancement device, $\lambda = 0$). Since $V_{DS} = V_{GS} > V_{GS} - V_{TH}$, it can never enter triode. Its small-signal resistance is $1/g_m$ (in parallel with r_o if one is given; body effect neglected), where $g_m = k_n V_{OV} = \sqrt{2k_n I_D} = 2I_D/V_{OV}$.

DIODE-CONNECTED BJT

$$V_{CB} = 0 \;\Rightarrow\; \text{active region}, \qquad I = I_C + I_B = I_C\left(1 + \frac{1}{\beta}\right), \qquad r \approx \frac{1}{g_m} = \frac{V_T}{I_C}$$

Base tied to collector. The collector junction has zero bias, so it is not forward biased and $I_C = \beta I_B$ still holds. The small-signal resistance is $r_\pi \parallel (1/g_m) \approx 1/g_m$ (hybrid-π model with $g_m = I_C/V_T$ and $r_\pi = \beta/g_m$), with thermal voltage $V_T \approx 25$ mV at room temperature (use 26 mV if the question does).

CURRENT MIRROR BUILT ON A DIODE-CONNECTED DEVICE

$$I_{out} = I_{ref}\frac{(W/L)_2}{(W/L)_1} \;\text{(MOSFET)}, \qquad I_{out} = \frac{I_{ref}}{1 + 2/\beta} \;\text{(matched BJTs)}$$

The diode-connected device sets V_{GS} (or V_{BE}) for a second device. The MOSFETs share V_{TH} and $\mu_n C_{ox}$ and differ only in W/L; the BJTs are identical (same I_S and β), so $I_{ref} = I_C + 2I_B$. Valid while the output device stays saturated (MOSFET) or active (BJT), with $\lambda = 0$ and the Early effect neglected.

DC POWER DISSIPATED IN THE DEVICE

$$P_D = V_{CE}I_C + V_{BE}I_B \approx V_{CE}I_C \;\text{(BJT)}, \qquad P_D = V_{DS}I_D \;\text{(MOSFET)}$$

Quiescent power turned into heat in the transistor. The base term is usually negligible. A MOSFET has no gate term because $I_G = 0$.

MAXIMUM DEVICE DISSIPATION ON A RESISTIVE LOAD LINE

$$P_{D,max} = \frac{V_{CC}^2}{4R} \quad \text{at} \quad V_{CE} = \frac{V_{CC}}{2},\ I_C = \frac{V_{CC}}{2R}$$

$R = R_C + R_E$ for a BJT (DC load line, $I_E \approx I_C$). For a MOSFET, replace V_{CC} by V_{DD}, V_{CE} by V_{DS} and I_C by I_D, with $R = R_D + R_S$. $P_D = I_C(V_{CC} - I_C R)$ is a parabola in I_C that peaks at the midpoint of the load line.

JUNCTION TEMPERATURE

$$T_J = T_A + \theta_{JA} P_D, \qquad P_{D,max} = \frac{T_{J,max} - T_A}{\theta_{JA}}$$

θ_{JA} is the thermal resistance from junction to ambient, in °C/W. With a heat sink, $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ (junction to case, case to sink, sink to ambient).

CONDITION FOR THERMAL STABILITY

$$\frac{\partial P_C}{\partial T_J} = \frac{\partial P_C}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_J} < \frac{1}{\theta_{JA}}$$

Dissipation must grow with junction temperature more slowly than the heat path can carry the extra heat away. Low stability factors keep $\partial I_C / \partial T_J$ small.

SELF-STABILISING Q-POINT

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C R = 2V_{CE} - V_{CC} < 0 \iff V_{CE} < \frac{V_{CC}}{2}$$

Here $P_C = V_{CE} I_C$ with $V_{CE} = V_{CC} - I_C R$ and $R = R_C + R_E$. With a Q-point below the midpoint of the load line, a rise in I_C lowers P_C, so runaway cannot start whatever the value of θ_{JA}.

Small-signal amplifiers, frequency response, current mirrors and differential amplifiers

BJT HYBRID-Π PARAMETERS

$$g_m = \frac{I_C}{V_T}, \qquad r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B}, \qquad r_e = \frac{\alpha}{g_m} = \frac{V_T}{I_E}, \qquad r_o = \frac{V_A}{I_C}$$

Active region, DC collector current I_C, Early voltage V_A. r_e is the resistance looking into the emitter with the base at AC ground (T-model), and $r_\pi = (\beta + 1) r_e$. Example: at $I_C = 1$ mA with $V_T = 25$ mV, $g_m = 40$ mA/V.

MOSFET SMALL-SIGNAL PARAMETERS

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ov} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{ov}}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}, \qquad g_{mb} = \chi g_m$$

NMOS in saturation, square law. The r_o expression uses $I_D(1 + \lambda V_{DS}) \approx I_D$. The gate draws no current, so the resistance looking into the gate is infinite. The body-effect transconductance g_{mb} matters only when a signal appears between source and body, as in CG and CD stages with the body tied to a rail. Its value depends on the DC source-body voltage through $\chi = \gamma / (2\sqrt{2\phi_F + V_{SB}})$. Neglect it unless the question gives γ, χ or g_{mb}.

INTRINSIC GAIN (THE MOST ONE TRANSISTOR CAN GIVE)

$$g_m r_\pi = \beta, \qquad g_m r_o\big|_{\text{BJT}} = \frac{V_A}{V_T}, \qquad g_m r_o\big|_{\text{MOS}} = \frac{2}{\lambda V_{ov}} = \frac{2V_A}{V_{ov}}$$

This is the magnitude of the gain of a CE/CS stage loaded only by its own r_o, as with an ideal current-source load. For a BJT it does not depend on the bias current.

H-PARAMETER (CE) EQUIVALENTS OF THE HYBRID-Π MODEL

$$h_{ie} = r_x + r_\pi \approx r_\pi, \qquad h_{fe} = \beta_0 = g_m r_\pi, \qquad h_{oe} = \frac{1}{r_o}, \qquad h_{re} \approx 0$$

Low-frequency CE h-parameters, defined by $v_{be} = h_{ie} i_b + h_{re} v_{ce}$ and $i_c = h_{fe} i_b + h_{oe} v_{ce}$. h_{re}, the reverse voltage feedback, is very small and is dropped in the approximate model.

TWO-PORT AMPLIFIER ANALYSIS WITH H-PARAMETERS (ANY CONFIGURATION)

$$A_I = \frac{I_L}{I_1} = \frac{-h_f}{1 + h_o Z_L}, \qquad Z_i = h_i + h_r A_I Z_L, \qquad A_V = \frac{A_I Z_L}{Z_i}, \qquad Y_o = h_o - \frac{h_f h_r}{h_i + R_{sig}}$$

I_1 enters the input terminal, I_2 enters the output terminal, and $I_L = -I_2$ flows into the load Z_L. R_{sig} is the source resistance. Y_o is the admittance looking back into the output terminals with the source set to zero. The gain from the source is $A_{Vs} = A_V \, Z_i/(Z_i + R_{sig})$. Use the h-parameters of the configuration in use (CE, CB or CC). The approximate CE result, with $h_{re} = 0$ and $h_{oe} Z_L \ll 1$, is $A_I \approx -h_{fe}$, $Z_i \approx h_{ie}$ and $A_V \approx -h_{fe} R_L / h_{ie}$.

RESISTANCE-REFLECTION RULES (BJT)

$$R_{\text{into base}} = r_\pi + (\beta + 1) R_{E,\text{tot}}, \qquad R_{\text{into emitter}} = \frac{r_\pi + R_{B,\text{tot}}}{\beta + 1} = r_e + \frac{R_{B,\text{tot}}}{\beta + 1}$$

$R_{E,\text{tot}}$ is the total AC resistance from emitter to ground. $R_{B,\text{tot}}$ is the total AC resistance from base to ground, i.e. the Thevenin resistance driving the base. r_o neglected. An impedance in the emitter looks $(\beta + 1)$ times larger from the base, and an impedance in the base looks $(\beta + 1)$ times smaller from the emitter.

RESISTANCE RULES (MOSFET)

$$R_{\text{into gate}} = \infty, \qquad R_{\text{into source}} = \frac{1}{g_m} \left(\frac{1}{g_m + g_{mb}} \text{ with body effect} \right)$$

Gate at AC ground, r_o neglected. No gate current flows, so any resistance in series with the gate carries no signal current. Including r_o and a drain load R_D gives $R_{\text{into source}} = (r_o + R_D)/[1 + (g_m + g_{mb}) r_o]$.

CE / CS VOLTAGE GAIN, WITH OR WITHOUT DEGENERATION

$$A_v = \frac{v_o}{v_b} = -\frac{\beta R'_L}{r_\pi + (\beta + 1) R_E} = -\frac{\alpha R'_L}{r_e + R_E} \approx -\frac{R'_L}{R_E}, \qquad A_v^{\text{MOS}} = -\frac{g_m R'_L}{1 + g_m R_S}$$

R_E (R_S) is the **unbypassed** emitter (source) resistance, and R'_L is the total AC load at the collector (drain). r_o and body effect neglected. With the emitter fully bypassed ($R_E = 0$) this reduces to $A_v = -g_m R'_L$. The approximation $-R'_L/R_E$ holds when $R_E \gg r_e$ ($g_m R_E \gg 1$), which makes the gain almost independent of β and temperature. The minus sign is a 180° phase inversion.

OVERALL GAIN FROM THE SIGNAL SOURCE

$$G_v = \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} A_v$$

R_{in} includes the bias network, e.g. $R_B \parallel r_\pi$. A_v is the loaded gain from the transistor's input terminal to the output.

OUTPUT RESISTANCE OF A DEGENERATED TRANSISTOR (R_O INCLUDED)

$$R_{out,C} = r_o \left[1 + g_m (R_E \parallel r_\pi)\right] + (R_E \parallel r_\pi) \approx r_o \left[1 + g_m (R_E \parallel r_\pi)\right], \qquad R_{out,D} = r_o + R_S + g_m r_o R_S \approx r_o (1 + g_m R_S)$$

Resistance looking into the collector (drain) with the base (gate) at AC ground and R_E (R_S) in the emitter (source). Body effect neglected; with it, $R_{out,D} = r_o + R_S + (g_m + g_{mb}) r_o R_S$. For a BJT it cannot exceed about $(\beta + 1) r_o$, reached when $R_E \gg r_\pi$. The stage's output resistance is $R_C \parallel R_{out,C}$. This result is the basis of the cascode and of improved current sources.

CS STAGE WITH A CURRENT-SOURCE OR DIODE-CONNECTED LOAD

$$A_v = -g_{m1}(r_{o1} \parallel r_{o2}) \text{ (current-source load)}, \qquad A_v = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} \text{ (diode-connected PMOS load)}$$

Q1 is the NMOS CS transistor and Q2 the PMOS load, both carrying the same I_D. With a current-source load (Q2's gate at a fixed bias), the drain node sees $r_{o1} \parallel r_{o2}$. With a diode-connected load, the drain sees about $1/g_{m2}$ (r_o neglected), so the gain is set by device sizes and is independent of bias. For a diode-connected NMOS load, replace μ_p by μ_n; with body effect on that load the gain is $-g_{m1}/(g_{m2} + g_{mb2})$.

SHORT-CIRCUIT TIME-CONSTANT METHOD

$$f_{p,i} = \frac{1}{2\pi C_i R_{i,s}}, \qquad f_L \approx \sum_i f_{p,i} = \frac{1}{2\pi} \sum_i \frac{1}{C_i R_{i,s}}$$

$R_{i,s}$ is the resistance seen by capacitor C_i with the signal source set to zero and all OTHER coupling and bypass capacitors short-circuited. When one pole is well above the rest, f_L is essentially that pole. When two poles are comparable, the sum overestimates f_L somewhat.

RESISTANCE SEEN BY EACH CAPACITOR (CE AND CS STAGES)

$$C_{C1}: \; R_{sig} + (R_B \parallel r_\pi)$$
$$C_{C2}: \; (R_C \parallel r_o) + R_L$$
$$C_E: \; R_E \parallel \left(r_e + \frac{R_{sig} \parallel R_B}{\beta + 1} \right)$$

CE stage whose emitter resistor is fully bypassed by C_E. For a CS stage: C_{C1} sees $R_{sig} + R_G$, C_{C2} sees $(R_D \parallel r_o) + R_L$, and the source bypass capacitor C_S sees $R_S \parallel (1/g_m)$.

BJT SHORT-CIRCUIT CURRENT GAIN, F_BETA AND F_T

$$h_{fe}(j\omega) = \frac{\beta_0}{1 + j\omega/\omega_\beta}, \qquad f_\beta = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)}, \qquad f_T = \beta_0 f_\beta = \frac{g_m}{2\pi (C_\pi + C_\mu)}$$

Collector AC-shorted to the emitter. The direct feed-through current of C_μ is neglected, which is valid for $\omega \ll g_m/C_\mu$. f_T is the frequency at which $|h_{fe}|$ falls to 1. For $f \gg f_\beta$, $|h_{fe}| \approx f_T/f$. If f_T and C_μ are given, $C_\pi = g_m/(2\pi f_T) - C_\mu$.

MOSFET UNITY-GAIN FREQUENCY

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

The frequency at which the short-circuit current gain $|i_d/i_g|$ equals 1.

MILLER'S THEOREM

$$Z_1 = \frac{Z}{1 - K}, \qquad Z_2 = \frac{Z}{1 - 1/K}; \qquad \text{for a capacitor: } C_1 = C(1 - K), \quad C_2 = C\left(1 - \frac{1}{K}\right)$$

An impedance Z connected between nodes 1 and 2, with $V_2 = KV_1$, can be replaced by Z_1 from node 1 to ground and Z_2 from node 2 to ground. The replacement is exact if K is the true ratio at the frequency considered. The Miller approximation uses the midband K. That is good for estimating the dominant input pole, but it loses the output pole and the zero.

MILLER INPUT CAPACITANCE AND F_H OF A CE / CS STAGE

$$C_{in} = C_\pi + C_\mu (1 + g_m R'_L), \qquad R_{\text{Th}} = r_\pi \parallel (r_x + R_{sig} \parallel R_B)$$
$$f_H \approx \frac{1}{2\pi R_{\text{Th}} C_{in}}$$

R_{Th} is the Thevenin resistance seen at the internal base node, across C_π ($r_x = 0$ under the convention above). $K = -g_m R'_L$ is the midband gain from base to collector. For a CS stage, $C_{in} = C_{gs} + C_{gd}(1 + g_m R'_L)$ and $R_{\text{Th}} = R_{sig} \parallel R_G$. On the output side, C_μ appears as $C_\mu[1 + 1/(g_m R'_L)] \approx C_\mu$.

OPEN-CIRCUIT TIME-CONSTANT ESTIMATE (CE / CS)

$$\omega_H \approx \frac{1}{\sum_i C_i R_{i,o}}, \qquad \tau_H = C_\pi R_{\mathrm{Th}} + C_\mu \left[R_{\mathrm{Th}}(1 + g_m R'_L) + R'_L\right] + C_L R'_L$$

$R_{i,o}$ is the resistance seen by C_i with all other device capacitors open and the source set to zero. C_L is any load capacitance at the output. The simple Miller estimate leaves out the $C_\mu R'_L$ and $C_L R'_L$ terms, so the Miller f_H comes out somewhat high. A CE/CS stage also has a right-half-plane zero at $\omega_z = g_m/C_\mu$ (g_m/C_{gd} for a MOSFET), usually far above f_H.

SINGLE-POLE AMPLIFIER AND GAIN-BANDWIDTH PRODUCT

$$A(s) = \frac{A_M}{1 + s/\omega_H}, \qquad \mathrm{GBW} = |A_M|\, f_H$$

At $f = f_H$ the gain is 3 dB down and the phase has shifted by −45° from its midband value. Above f_H the gain of a single-pole amplifier falls at 20 dB/decade and reaches unity at GBW. For a single-pole amplifier with frequency-independent negative feedback, reducing the midband gain by the factor (1 + loop gain) raises f_H by the same factor, so GBW stays constant.

STEP AND SQUARE-WAVE RESPONSE

$$t_r = 2.2\tau = \frac{2.2}{2\pi f_H} \approx \frac{0.35}{f_H}, \qquad P \approx \frac{\pi f_L}{f} \times 100\%$$

t_r is the 10–90% rise time of the step response of a single-pole low-pass amplifier with $\tau = 1/(2\pi f_H)$. P is the percentage tilt (sag) of a square wave of frequency f passed through a single-pole high-pass response with cut-off f_L, valid when the tilt is small ($f \gg f_L$).

CASCADE GAIN

$$A_v = A_{v1} A_{v2} \cdots A_{vn}, \qquad 20\log_{10}|A_v| = \sum_k 20\log_{10}|A_{vk}|, \qquad A_{vk} \text{ with load } R_{C,k} \parallel R_{in,k+1}$$

Use loaded gains, not open-circuit gains. Signs multiply: two inverting stages give a non-inverting cascade.

BANDWIDTH OF N IDENTICAL NON-INTERACTING STAGES

$$f_H^{(n)} = f_H \sqrt{2^{1/n} - 1}, \qquad f_L^{(n)} = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

Each stage has a single high-frequency pole at f_H (and a single low-frequency pole at f_L), and the stages do not shift each other's poles. $\sqrt{2^{1/n} - 1}$ is 0.644 for $n = 2$ and 0.510 for $n = 3$, so cascading narrows the bandwidth at both ends.

CASCODE: OUTPUT RESISTANCE AND GAIN

$$R_{out}^{\mathrm{BJT}} \approx r_{o2}\left[1 + g_{m2}(r_{o1} \parallel r_{\pi 2})\right] \approx \beta r_o$$
$$R_{out}^{\mathrm{MOS}} \approx g_{m2} r_{o2} r_{o1}$$
$$A_v \approx -g_{m1}(R_{out} \parallel R_L)$$

Q1 (CE/CS) drives the emitter/source of Q2 (CB/CG), and R_L is the total load at Q2's collector/drain. The βr_o limit (strictly $(\beta + 1) r_o$) assumes $r_{o1} \gg r_{\pi 2}$. Body effect neglected; with it, $g_{m2} \to g_{m2} + g_{mb2}$ in the MOS result. In a BJT cascode (r_o neglected) the resistance looking into Q2's emitter is about $1/g_{m2}$. Q1's own gain is then about $-g_{m1}/g_{m2} = -1$ at equal currents, and its C_μ is Miller-multiplied by only about 2. In a MOS cascode the resistance into Q2's source is $(r_{o2} + R_L)/(1 + g_{m2} r_{o2})$. That is close to $1/g_{m2}$ only when $R_L \ll r_{o2}$; with a high-resistance load the Miller factor on Q1's C_{gd} is larger. With an ideal current-source load, the MOS cascode gain magnitude is about $(g_m r_o)^2$.

REFERENCE CURRENT

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R}\ (\mathrm{BJT}), \qquad I_{REF} = \frac{V_{DD} - V_{GS}}{R} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{th})^2\ (\mathrm{MOS})$$

Diode-connected transistor at the ground rail, fed through R from the supply. For the MOSFET, solve the two equations together for V_{GS} and keep the root with $V_{GS} > V_{th}$.

BASIC BJT MIRROR WITH FINITE B

$$I_O = \frac{I_{REF}}{1 + 2/\beta}; \qquad Q_2 \text{ with } m \text{ times the area of } Q_1: \; I_O = \frac{m\, I_{REF}}{1 + (m+1)/\beta}$$

Matched devices, Early effect neglected. With N identical outputs driven from one diode, each output carries $I_{REF}/[1 + (N+1)/\beta]$.

MOSFET MIRROR

$$I_O = I_{REF}\,\frac{(W/L)_2}{(W/L)_1}\;(\lambda = 0), \qquad I_O = I_{REF}\,\frac{(W/L)_2}{(W/L)_1}\cdot\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{GS}}$$

There is no gate current, so there is no β-type error. The only errors come from the V_{DS} difference (through λ) and from device mismatch. Q2 must stay saturated: $V_{DS2} \geq V_{ov}$. The output resistance is $R_o = r_{o2}$.

EARLY EFFECT IN A BJT MIRROR; OUTPUT RESISTANCE

$$I_O \approx \frac{I_{REF}}{1 + 2/\beta}\left(1 + \frac{V_O - V_{BE}}{V_A}\right), \qquad R_o = r_{o2} = \frac{V_A}{I_O}$$

V_O is Q2's collector voltage. The copy is exact only when $V_O = V_{BE}$, i.e. when Q2 has the same V_{CE} as the diode-connected Q1.

WIDLAR CURRENT SOURCE

$$V_T \ln\frac{I_{REF}}{I_O} = I_O R_E, \qquad R_o \approx r_{o2}\,[1 + g_{m2}(R_E \parallel r_{\pi 2})]$$

A resistor R_E sits in Q2's emitter only. Matched devices, base currents neglected, so $I_{C1} \approx I_{REF}$. $g_{m2} = I_O/V_T$ and $r_{\pi 2} = \beta/g_{m2}$. It gives a small I_O (microamps) with moderate resistor values. For a design (I_O given), solve directly for R_E. For an analysis (R_E given), iterate.

WILSON CURRENT MIRROR

$$\frac{I_O}{I_{REF}} = 1 - \frac{2}{\beta^2 + 2\beta + 2} \approx 1 - \frac{2}{\beta^2}, \qquad R_o \approx \frac{\beta r_o}{2}$$

BJT version. Negative feedback through the third transistor cancels the base-current error to first order and raises R_o. The MOS Wilson mirror gives $I_O = I_{REF}$ (matched, $\lambda = 0$) and $R_o \approx g_m r_o^2$.

CASCODE CURRENT MIRROR

$$R_o^{\text{BJT}} \approx \beta r_o, \qquad R_o^{\text{MOS}} \approx g_{m3} r_{o3} r_{o2} \approx g_m r_o^2$$

A second, stacked mirror holds the output transistor's emitter (source) at a nearly fixed voltage. The output therefore looks into a degenerated transistor, as in the cascode rule. Cost: the output needs about $V_{BE} + V_{CE,sat}$ (BJT) or $V_{th} + 2V_{ov}$ (MOS) above the rail. BJT ratio: $I_O \approx I_{REF}/(1 + 4/\beta)$.

OUTPUT OF A DIFFERENTIAL AMPLIFIER; CMRR

$$v_o = A_d v_{id} + A_{cm} v_{icm}, \qquad \text{CMRR} = \left|\frac{A_d}{A_{cm}}\right|, \qquad \text{CMRR (dB)} = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right|$$

Valid for any linear two-input amplifier. A_d and A_{cm} must refer to the same output, either single-ended or differential.

LARGE-SIGNAL TRANSFER CHARACTERISTICS

$$i_{C1} = \frac{\alpha I}{1 + e^{-v_{id}/V_T}}, \qquad i_{C2} = \frac{\alpha I}{1 + e^{v_{id}/V_T}}$$

$$i_{D1,2} = \frac{I}{2} \pm \frac{I}{V_{ov}}\,\frac{v_{id}}{2}\sqrt{1 - \left(\frac{v_{id}/2}{V_{ov}}\right)^2}, \qquad |v_{id}| \leq \sqrt{2}\,V_{ov}$$

BJT: roughly linear only for $|v_{id}| \ll 2V_T$, and about $4V_T$ (≈ 100 mV) steers 98% of the tail current to one side. MOSFET (square law, V_{ov} at balance): all of I flows in one transistor once $|v_{id}| \geq \sqrt{2}\,V_{ov}$, and small-signal operation needs $|v_{id}|/2 \ll V_{ov}$. The two currents always add up to I (αI for the BJT).

DIFFERENTIAL GAIN WITH RESISTIVE LOADS

$$A_d = \frac{v_{c1} - v_{c2}}{v_{id}} = -g_m R_C \text{ (differential output)}, \qquad A_d = \mp\frac{g_m R_C}{2} \text{ (single-ended at } C_1 \text{ / } C_2)$$

Add $\| \, r_o$ to R_C when r_o is given. A load R_L connected between the two collectors appears as $R_L/2$ in each half-circuit. With a resistor R_E in each emitter, the differential-output gain becomes $-\alpha R_C/(r_e + R_E)$ (half that single-ended). The differential input resistance is $R_{id} = 2r_\pi$ for a BJT pair, $2(\beta+1)(r_e + R_E)$ with a resistor R_E in each emitter, and infinite for MOSFETs. For MOSFETs replace R_C by R_D.

COMMON-MODE GAIN AND CMRR WITH RESISTIVE LOADS

$$A_{cm} = -\frac{\alpha R_C}{r_e + 2R_{EE}} \approx -\frac{R_C}{2R_{EE}} \text{ (single-ended)}$$

$$\text{CMRR}_{\text{single-ended}} = \frac{1}{2} + \frac{g_m R_{EE}}{\alpha} \approx g_m R_{EE}$$

$$\text{CMRR}_{\text{diff. output}} \approx \frac{2g_m R_{EE}}{\Delta R_C / R_C} \text{ (load mismatch } \Delta R_C)$$

Comes from the common-mode half-circuit with $2R_{EE}$ in each emitter; r_o of the pair neglected. The approximations assume $\alpha \approx 1$ and $g_m R_{EE} \gg 1$; with $\alpha = 1$ the single-ended CMRR is $(1 + 2g_m R_{EE})/2$. With differential output and perfect matching, $A_{cm} = 0$. A load-resistor mismatch ΔR_C gives $|A_{cm}| = \Delta R_C/(2R_{EE})$. MOSFET: replace R_{EE} by R_{SS}, r_e by $1/g_m$, R_C by R_D, and drop α. The single-ended CMRR is then exactly $(1 + 2g_m R_{SS})/2$.

ACTIVE (CURRENT-MIRROR) LOAD

$$A_d = \frac{v_o}{v_{id}} = g_m(r_{o2} \parallel r_{o4}), \qquad R_o = r_{o2} \parallel r_{o4}, \qquad A_{cm}^{\text{MOS}} \approx -\frac{1}{2g_{m3}R_{SS}}, \qquad \text{CMRR}^{\text{MOS}} \approx g_m(r_{o2} \parallel r_{o4})(2g_{m3}R_{SS})$$

Q1–Q2 form the pair and Q3 (diode-connected)–Q4 form the mirror load. The output is single-ended at the Q2–Q4 node, with no external load. The mirror adds Q1's signal current to Q2's, so the single-ended output gets the full g_m rather than $g_m/2$. With equal r_o, $A_d = g_m r_o/2$; for a BJT pair with equal V_A this is $V_A/(2V_T)$. g_{m3} is the transconductance of the diode-connected mirror transistor, and the A_{cm} result assumes $2g_m R_{SS} \gg 1$.

INPUT COMMON-MODE RANGE

$$\text{BJT: } -V_{EE} + V_{CS,min} + V_{BE} \le v_{ICM} \le V_{CC} - \frac{\alpha I}{2} R_C$$

$$\text{MOS: } -V_{SS} + V_{CS,min} + V_{th} + V_{ov} \le v_{ICM} \le V_{DD} - \frac{I}{2} R_D + V_{th}$$

$V_{CS,min}$ is the smallest voltage across which the tail current source still behaves as a current source. The upper limit keeps the pair active. For the BJT it is written with $V_{CB} \ge 0$; some texts allow up to about 0.4 V of forward base-collector bias, which raises the limit by that much. For the MOSFET it is $V_{DS} \ge V_{ov}$, i.e. $V_D \ge V_G - V_{th}$.

Feedback amplifiers and oscillators

CLOSED-LOOP GAIN (NEGATIVE FEEDBACK)

$$A_f = \frac{x_o}{x_s} = \frac{A}{1 + A\beta}$$

Convention: $x_i = x_s - x_f$, $x_f = \beta x_o$. The feedback is negative when $A\beta > 0$ in the mid-band (in general, when $|1 + A\beta| > 1$).

LOOP GAIN AND AMOUNT OF FEEDBACK

$$T = A\beta, \qquad D = 1 + A\beta, \qquad \text{gain reduction} = 20\log_{10}|1 + A\beta| \text{ dB}$$

T is the gain once round the loop. Every benefit of negative feedback, and the loss of gain, is by the factor D.

LARGE LOOP GAIN

$$A_f \approx \frac{1}{\beta} \quad (A\beta \gg 1)$$

Exact form: $A_f = \frac{1}{\beta} \cdot \frac{A\beta}{1+A\beta}$. So $1/\beta$ overstates the true gain by the fraction $1/(A\beta)$; equivalently, the true gain lies below $1/\beta$ by the fraction $1/(1+A\beta)$.

DESENSITIVITY TO THE AMPLIFIER GAIN

$$\frac{dA_f}{A_f} = \frac{1}{1+A\beta} \cdot \frac{dA}{A}$$

A differential result, valid for small changes in A with β fixed; $1+A\beta$ is also called the desensitivity factor. For a large change, work out A_f exactly before and after.

UPPER CUTOFF WITH FEEDBACK

$$A_{Mf} = \frac{A_M}{1+A_M\beta}, \qquad \omega_{Hf} = \omega_H\,(1+A_M\beta)$$

Amplifier with a single high-frequency pole ω_H and mid-band gain A_M; β independent of frequency.

LOWER CUTOFF WITH FEEDBACK

$$\omega_{Lf} = \frac{\omega_L}{1+A_M\beta}$$

Single low-frequency pole, $A(s) = A_M/(1+\omega_L/s)$; β independent of frequency.

GAIN-BANDWIDTH PRODUCT

$$A_{Mf}\,\omega_{Hf} = A_M\,\omega_H$$

Constant for a single-pole amplifier: gain is traded one-for-one for bandwidth. It is not exact when the amplifier has more than one significant pole.

DISTORTION AND NOISE GENERATED INSIDE THE LOOP

$$V_{d,f} = \frac{V_d}{1+A\beta}, \qquad V_{n,f} = \frac{V_n}{1+A\beta}$$

V_d and V_n are the distortion and noise components at the output without feedback, generated inside the loop after the input (for example in the output stage). $V_{d,f}$ and $V_{n,f}$ are the same components with feedback, compared at the same output signal amplitude.

INPUT RESISTANCE, SERIES MIXING

$$R_{if} = R_i\,(1+A\beta)$$

The feedback voltage is in series with the source. R_i is the input resistance of the basic amplifier.

INPUT RESISTANCE, SHUNT MIXING

$$R_{if} = \frac{R_i}{1+A\beta}$$

The feedback current is added at the input node.

OUTPUT RESISTANCE, VOLTAGE (SHUNT) SAMPLING

$$R_{of} = \frac{R_o}{1+A\beta}$$

Here A is the open-circuit (load removed) gain of the basic amplifier, because its output is modelled as a Thevenin source.

OUTPUT RESISTANCE, CURRENT (SERIES) SAMPLING

$$R_{of} = R_o\,(1 + A\beta)$$

Here A is the short-circuit (load shorted) gain of the basic amplifier, because its output is modelled as a Norton source.

CE STAGE WITH UNBYPASSED EMITTER RESISTOR

$$A_v = \frac{v_o}{v_s} = -\frac{h_{fe}R_C}{r_\pi + (1 + h_{fe})R_E} \approx -\frac{R_C}{R_E}$$

Series-series feedback. Hybrid-π model with $g_m = I_C/V_T$ ($V_T = 25\,\text{mV}$ at room temperature if a number is needed) and $r_\pi = h_{fe}/g_m$; the current gain is written h_{fe} to keep β for the feedback factor; r_o neglected; no source resistance; output at the collector, with R_C the total collector load. The approximation holds when $(1 + h_{fe})R_E \gg r_\pi$ and $h_{fe} \gg 1$. Input resistance looking into the base: $r_\pi + (1 + h_{fe})R_E$.

BARKHAUSEN CRITERION

$$A(j\omega_0)\,\beta(j\omega_0) = 1 \;\Leftrightarrow\; |A\beta| = 1 \;\text{ and }\; \angle A\beta = 360^\circ n \;\; (n = 0, 1, 2, \dots)$$

The steady-state condition for a linear, sinusoidal oscillation at ω_0 (positive-feedback convention). The phase condition fixes ω_0, and the magnitude condition fixes the minimum gain. For reliable start-up the small-signal $|A\beta|$ is made slightly greater than 1.

OP-AMP RC PHASE-SHIFT OSCILLATOR

$$f_0 = \frac{1}{2\pi\sqrt{6}\,RC}, \qquad \beta(f_0) = -\frac{1}{29}, \qquad R_f \geq 29R$$

Three identical high-pass sections, ideal op-amp, third R being the inverting amplifier's input resistor. The inverting gain magnitude R_f/R must be at least 29.

LOW-PASS LADDER (SERIES R, SHUNT C)

$$f_0 = \frac{\sqrt{6}}{2\pi RC}, \qquad \beta(f_0) = -\frac{1}{29}$$

Three identical low-pass sections under the same conditions (zero-impedance drive, unloaded output). The minimum inverting gain is still 29.

THREE BUFFERED (NON-INTERACTING) RC SECTIONS

$$f_0 = \frac{1}{2\pi\sqrt{3}\,RC}\;(\text{high-pass}), \qquad f_0 = \frac{\sqrt{3}}{2\pi RC}\;(\text{low-pass}), \qquad \beta(f_0) = -\frac{1}{8}$$

Each section is isolated by an ideal buffer, so it does not load the one before it. Each then supplies exactly 60° at f_0 and attenuates by $\cos 60^\circ = 1/2$, so the three give $(1/2)^3 = 1/8$ and the inverting amplifier needs a gain magnitude of at least 8.

WIEN NETWORK, GENERAL COMPONENTS

$$\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}}, \qquad \beta(\omega_0) = \frac{1}{1 + \dfrac{R_1}{R_2} + \dfrac{C_2}{C_1}}$$

R_1 and C_1 form the series arm; R_2 and C_2 (in parallel) form the shunt arm, across which the output is taken. The phase of β is zero at ω_0. Minimum non-inverting gain: $1/\beta(\omega_0)$.

WIEN BRIDGE, EQUAL COMPONENTS

$$f_0 = \frac{1}{2\pi RC}, \qquad \beta(f_0) = \frac{1}{3}, \qquad A = 1 + \frac{R_f}{R_g} \geq 3 \;\; (R_f \geq 2R_g)$$

$R_1 = R_2 = R$ and $C_1 = C_2 = C$, with an ideal non-inverting op-amp amplifier.

THREE-REACTANCE (LC) OSCILLATOR

$$X_o + X_i + X_f = 0, \qquad \beta = -\frac{X_i}{X_o}, \qquad |A_v|_{\min} = \frac{X_o}{X_i}$$

Pure (lossless) reactances. X_o and X_i must be the same kind of reactance, and X_f the opposite kind. Two capacitors and an inductor make a Colpitts oscillator; two inductors and a capacitor make a Hartley oscillator.

COLPITTS OSCILLATOR

$$f_0 = \frac{1}{2\pi\sqrt{L\,C_{eq}}}, \qquad C_{eq} = \frac{C_1 C_2}{C_1 + C_2}, \qquad |A_v| \geq \frac{C_2}{C_1}$$

C_1 runs from the amplifier output to ground, C_2 from the amplifier input to ground, and L between them; $\beta = -C_1/C_2$. The required gain is (input-side capacitance)/(output-side capacitance).

HARTLEY OSCILLATOR

$$f_0 = \frac{1}{2\pi\sqrt{(L_1 + L_2 + 2M)\,C}}, \qquad |A_v| \geq \frac{L_1 + M}{L_2 + M}$$

L_1 is on the output side, L_2 on the input side, and C is across both; M is the mutual inductance of a tapped coil (aiding). For separate, uncoupled coils put $M = 0$, which gives $|A_v| \geq L_1/L_2$.

CRYSTAL: SERIES RESONANCE

$$f_s = \frac{1}{2\pi\sqrt{L\,C_s}}, \qquad Q = \frac{\omega_s L}{R} = \frac{1}{\omega_s C_s R}$$

Resonance of the motional arm alone; here the crystal's impedance is at its minimum (resistive, equal to R). Q is the quality factor of the motional arm, with $\omega_s = 2\pi f_s$.

CRYSTAL: PARALLEL RESONANCE

$$f_p = \frac{1}{2\pi\sqrt{L\,\dfrac{C_s C_p}{C_s + C_p}}} = f_s\sqrt{1 + \frac{C_s}{C_p}} \approx f_s\left(1 + \frac{C_s}{2C_p}\right)$$

The motional arm resonating with C_s in series with C_p; here the crystal's impedance is at its maximum. The approximation uses $C_s \ll C_p$.

OP-AMP SQUARE-WAVE GENERATOR

$$T = 2RC\ln\left(\frac{1+\beta}{1-\beta}\right), \qquad \beta = \frac{R_1}{R_1 + R_2}, \qquad f = \frac{1}{T}$$

Ideal op-amp whose output saturates symmetrically at $\pm V_{sat}$ and switches instantly. Each half-period is $RC\ln[(1+\beta)/(1-\beta)]$: the capacitor starts at $\mp\beta V_{sat}$ and charges towards $\pm V_{sat}$. With $R_1 = R_2$, $\beta = 1/2$ and $T = 2RC\ln 3 \approx 2.197\,RC$. The duty cycle is 50%; with unequal saturation levels the two half-periods differ.

Op-amp circuits: characteristics, applications and compensation

OPEN-LOOP RELATION AND VIRTUAL SHORT

$$v_o = A\,(v_+ - v_-), \qquad v_+ - v_- = \frac{v_o}{A} \to 0 \text{ as } A \to \infty$$

The input difference goes to zero only when negative feedback holds the output at a finite value inside $\pm V_{sat}$.

INVERTING AMPLIFIER

$$\frac{v_o}{v_i} = -\frac{R_f}{R_1}, \qquad R_{in} = R_1, \qquad R_{out} = 0$$

The input goes through R_1 to the virtual-ground node, so the source sees only R_1.

NON-INVERTING AMPLIFIER AND VOLTAGE FOLLOWER

$$\frac{v_o}{v_i} = 1 + \frac{R_f}{R_1}, \qquad R_{in} \to \infty$$

The input is at v_+, with R_1 from v_- to ground. The gain is never below 1. With $R_f = 0$ or $R_1 \to \infty$ this is the voltage follower, $v_o = v_i$, used as a buffer.

INVERTING SUMMER

$$v_o = -R_f \left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \cdots + \frac{v_n}{R_n} \right)$$

Each input sees only its own resistor because the summing node is a virtual ground, so the inputs do not interact. With all resistors equal, $v_o = -(v_1 + \cdots + v_n)$.

DIFFERENCE AMPLIFIER (GENERAL)

$$v_o = -\frac{R_2}{R_1} v_1 + \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3 + R_4} v_2$$

v_1 goes through R_1 to v_-, with R_2 from the output to v_-; v_2 goes through R_3 to v_+, with R_4 from v_+ to ground. The result follows by superposition.

BALANCED DIFFERENCE AMPLIFIER

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} \;\Rightarrow\; v_o = \frac{R_2}{R_1}(v_2 - v_1)$$

The common-mode input cancels only with this ratio match. The differential input resistance is $2R_1$ when $R_3 = R_1$ and $R_4 = R_2$; v_2 alone sees $R_3 + R_4$.

THREE-OP-AMP INSTRUMENTATION AMPLIFIER

$$v_o = \left(1 + \frac{2R}{R_G}\right) \frac{R_4}{R_3} (v_2 - v_1)$$

v_2 drives the op-amp whose output feeds the non-inverting side of the difference stage. The gain is set by the single resistor R_G without disturbing the matched R_3 and R_4. The first-stage outputs are $v_{o1} = v_1 - R(v_2 - v_1)/R_G$ and $v_{o2} = v_2 + R(v_2 - v_1)/R_G$.

IDEAL INVERTING INTEGRATOR

$$v_o(t) = -\frac{1}{RC} \int_0^t v_i(\tau)\, d\tau + v_o(0), \qquad H(j\omega) = -\frac{1}{j\omega RC}$$

$|H| = 1$ at $\omega = 1/(RC)$ and falls at 20 dB/decade. The phase is $+90^\circ$ (the output leads the input). The DC gain is infinite.

PRACTICAL INTEGRATOR (RF ACROSS C)

$$H(j\omega) = -\frac{R_f/R}{1 + j\omega R_f C}$$

It integrates only for $f \gg f_c = 1/(2\pi R_f C)$. Below f_c it is an inverting amplifier of gain $-R_f/R$, which stops offsets and bias currents from ramping the output into saturation.

IDEAL DIFFERENTIATOR

$$v_o(t) = -RC \frac{dv_i}{dt}, \qquad H(j\omega) = -j\omega RC$$

$|H| = 1$ at $\omega = 1/(RC)$, and the gain rises at 20 dB/decade without limit. The phase is -90° (the output lags the input).

PRACTICAL DIFFERENTIATOR (R1 IN SERIES WITH C)

$$H(j\omega) = -\frac{j\omega RC}{1 + j\omega R_1 C}$$

It differentiates only for $f \ll 1/(2\pi R_1 C)$, and the high-frequency gain is capped at $-R/R_1$. A small capacitor across R is sometimes added to roll the gain off further.

INTEGRATOR OUTPUT FOR A SQUARE-WAVE INPUT

$$\Delta v_{o,pp} = \frac{V_m\, T}{2RC}$$

For a zero-average square wave of $\pm V_m$ and period T, the output slopes at $\mp V_m/(RC)$ for $T/2$ each half-cycle. A practical integrator needs $R_f C \gg T$ for this to hold.

IMPROVED PRECISION HALF-WAVE RECTIFIER (DIODES AS DESCRIBED)

$$v_o = \begin{cases} -\dfrac{R_2}{R_1}\, v_i, & v_i < 0 \\ 0, & v_i > 0 \end{cases}$$

Reversing both diodes passes the other half-cycle: $v_o = -(R_2/R_1)v_i$ for $v_i > 0$ and 0 otherwise. The op-amp output stays within about one diode drop of ground (while D_1 conducts) or of the output node (while D_2 conducts), so it never saturates and there is no saturation recovery.

PRECISION FULL-WAVE RECTIFIER

$$v_o = -(v_i + 2v_A) = |v_i|$$

For $v_i > 0$: $v_A = -v_i$, so $v_o = -(v_i - 2v_i) = v_i$. For $v_i < 0$: $v_A = 0$, so $v_o = -v_i$. Reversing both diodes gives $-|v_i|$.

LOG AMPLIFIER

$$v_o = -V_T \ln\left(\frac{v_i}{I_S R}\right), \qquad v_i > 0$$

It works for one input polarity only (reverse the diode for $v_i < 0$). The output depends on temperature through both V_T and I_S. With a BJT (collector at v_-, base grounded, emitter at the output), I_S is the transistor's saturation current.

ANTILOG AMPLIFIER

$$v_o = -I_S R\, e^{v_i/V_T}, \qquad v_i > 0$$

The diode (anode at the input) is in series with the input, and R is in the feedback path.

CLOSED-LOOP GAIN WITH FINITE OPEN-LOOP GAIN (NON-INVERTING)

$$G = \frac{A}{1 + A\beta} = \frac{1}{\beta} \cdot \frac{A\beta}{1 + A\beta}, \qquad \beta = \frac{R_1}{R_1 + R_f}$$

The op-amp is ideal except for its finite gain A ($R_i \to \infty$, $R_o = 0$). $A\beta$ is the loop gain. As $A \to \infty$, $G \to 1/\beta = 1 + R_f/R_1$.

CLOSED-LOOP GAIN WITH FINITE OPEN-LOOP GAIN (INVERTING)

$$G = \frac{-R_f/R_1}{1 + \dfrac{1 + R_f/R_1}{A}}$$

The loop gain is the same $A\beta$ with the same $\beta = R_1/(R_1 + R_f)$. The virtual ground now sits at $-v_o/A$ rather than exactly 0.

FRACTIONAL GAIN ERROR

$$\varepsilon = \frac{G_{\text{ideal}} - G}{G_{\text{ideal}}} = \frac{1}{1 + A\beta} \approx \frac{1 + R_f/R_1}{A}$$

This holds for both configurations; the approximation needs $A\beta \gg 1$. A higher closed-loop gain means a smaller loop gain and a larger error.

INTERNALLY COMPENSATED OP-AMP (SINGLE POLE)

$$A(j\omega) = \frac{A_0}{1 + j\omega/\omega_b}, \qquad \omega_t = A_0\,\omega_b$$

ω_b is the open-loop 3-dB frequency. For $A_0 \gg 1$, $f_t = A_0 f_b$ is the unity-gain frequency, also called the gain-bandwidth product (GBW). For $\omega \gg \omega_b$, $|A| \approx \omega_t/\omega$.

CLOSED-LOOP BANDWIDTH

$$f_{3\text{dB}} = f_b(1 + A_0\beta) \approx \beta f_t = \frac{f_t}{1 + R_f/R_1}$$

This is the same for inverting and non-inverting amplifiers built with the same resistors: the bandwidth is f_t divided by the noise gain.

GAIN-BANDWIDTH PRODUCT IN EACH CONFIGURATION

$$\text{non-inverting: } G_0 f_{3\text{dB}} = f_t, \qquad \text{inverting: } \frac{R_f}{R_1}\, f_{3\text{dB}} = \frac{R_f/R_1}{1 + R_f/R_1}\, f_t$$

An inverting amplifier of gain -1 has a bandwidth of $f_t/2$, not f_t.

SMALL-SIGNAL RISE TIME (10% TO 90%)

$$t_r = 2.2\,\tau = \frac{2.2}{2\pi f_{3\text{dB}}} \approx \frac{0.35}{f_{3\text{dB}}}$$

Applies to a single-pole closed-loop response to a small step.

SLEW RATE

$$SR = \left.\frac{dv_o}{dt}\right|_{\max}, \qquad \omega V_p \le SR \text{ for an undistorted sine } V_p \sin \omega t$$

This is a large-signal limit on the output and does not depend on the closed-loop gain. A heavily slew-limited sine approaches a triangle, and a large step becomes a ramp of slope SR.

FULL-POWER BANDWIDTH

$$f_M = \frac{SR}{2\pi V_{o,\max}}$$

The highest frequency at which a sine at the full rated output amplitude $V_{o,\max}$ is undistorted. Above f_M the amplitude must drop to $SR/(2\pi f)$.

OUTPUT OFFSET DUE TO INPUT OFFSET VOLTAGE

$$V_o = V_{OS}\left(1 + \frac{R_f}{R_1}\right)$$

This is the same for inverting and non-inverting amplifiers. In an integrator without R_f, V_{OS} makes the output ramp at $V_{OS}/(RC)$, and the bias current I_{B1} makes it ramp at I_{B1}/C.

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT

$$I_B = \frac{I_{B1} + I_{B2}}{2}, \qquad I_{OS} = |I_{B1} - I_{B2}|$$

Here both currents are taken as flowing into the input terminals.

OUTPUT ERROR DUE TO BIAS CURRENTS

$$V_o = I_{B1}R_f \text{ (no compensation)}, \qquad V_o = R_f(I_{B1} - I_{B2}) \text{ with } R_3 = R_1 \parallel R_f \text{ at } v_+$$

Signal sources are replaced by their resistances (zero for an ideal source; in the inverting amplifier any source resistance is part of R_1). Without R_3 the non-inverting input sits at 0 V, so no current flows in R_1 and all of I_{B1} flows through R_f. Choosing $R_3 = R_1 \parallel R_f$ makes the two bias currents see equal resistances, which leaves only $|V_o| = I_{OS}R_f$. R_3 does nothing about V_{OS}.

COMMON-MODE REJECTION RATIO

$$\mathrm{CMRR} = \left|\frac{A_d}{A_{cm}}\right|, \qquad \mathrm{CMRR}_{\mathrm{dB}} = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right|$$

Applies to the bare op-amp and to a whole difference or instrumentation amplifier. For a circuit, A_d and A_{cm} are its gains to $v_2 - v_1$ and to $(v_1 + v_2)/2$.

PHASE MARGIN

$$\mathrm{PM} = 180^\circ + \angle L(j\omega_c), \qquad |L(j\omega_c)| = 1$$

ω_c is the loop-gain crossover frequency. PM > 0 means the loop is stable. A small PM shows up as peaking in the frequency response and ringing in the step response.

GAIN MARGIN

$$\mathrm{GM} = -20\log_{10}|L(j\omega_{180})|\ \mathrm{dB}, \qquad \angle L(j\omega_{180}) = -180^\circ$$

A positive GM (in dB) means the loop is stable.

PHASE MARGIN OF A TWO-POLE LOOP

$$\mathrm{PM} = 90^\circ - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \quad (\omega_{p1} \ll \omega_c)$$

ω_c is the true crossover frequency. $\omega_c = \omega_{p2}$ gives 45°, $\omega_c = \omega_{p2}/\sqrt{3}$ gives 60°, and $\omega_c = \omega_{p2}/2$ gives 63.4°.

MILLER CAPACITANCE AT THE FIRST-STAGE OUTPUT

$$C_M = C_c\,(1 + G_{m2}R_2)$$

Any capacitance bridging an inverting voltage gain $-A_2$ appears at the input as $C(1 + A_2)$.

DOMINANT POLE WITH MILLER COMPENSATION

$$\omega_{p1} \approx \frac{1}{R_1 C_c\, G_{m2} R_2}$$

Assumes $G_{m2}R_2 \gg 1$ and $C_c G_{m2} R_2 \gg C_1$.

UNITY-GAIN FREQUENCY OF A MILLER-COMPENSATED OP-AMP

$$\omega_t = A_0\,\omega_{p1} = \frac{G_{m1}}{C_c}$$

Set only by C_c and the input-stage transconductance.

NON-DOMINANT POLE AFTER POLE SPLITTING

$$\omega_{p2} \approx \frac{G_{m2}C_c}{C_1C_2 + C_c(C_1 + C_2)} \approx \frac{G_{m2}}{C_2}$$

The second form needs $C_1 \ll C_c$ and $C_1 \ll C_2$. Keeping $\omega_t \le \omega_{p2}$ in a follower requires $C_c \ge G_{m1}C_2/G_{m2}$.

SLEW RATE OF A MILLER-COMPENSATED OP-AMP

$$SR = \frac{I}{C_c} = \omega_t\,\frac{I}{G_{m1}}$$

I is the tail current of the input differential pair, the most current available to charge C_c. For a BJT input pair ($G_{m1} = I/(2V_T)$), $SR = 2V_T\,\omega_t$. For a MOSFET input pair ($G_{m1} = I/V_{ov}$), $SR = V_{ov}\,\omega_t$.

Active filters, comparators, Schmitt triggers, timers, VCOs and PLLs

FIRST-ORDER LOW-PASS, NON-INVERTING

$$H(s) = \frac{V_o}{V_i} = \frac{A_0}{1 + sRC}, \qquad A_0 = 1 + \frac{R_f}{R_1}, \qquad f_c = \frac{1}{2\pi RC}$$

R in series from the input to the + terminal, C from the + terminal to ground; R_1 (– terminal to ground) and R_f (output to – terminal) set the passband gain and do not affect f_c. $|H(jf)| = A_0/\sqrt{1 + (f/f_c)^2}$ and $\angle H = -\tan^{-1}(f/f_c)$. With $R_f = 0$ (voltage follower), $A_0 = 1$.

FIRST-ORDER HIGH-PASS, NON-INVERTING

$$H(s) = \frac{A_0\, sRC}{1 + sRC}, \qquad f_c = \frac{1}{2\pi RC}$$

R and C swap places: C in series to the + terminal, R from the + terminal to ground. $|H(jf)| = A_0(f/f_c)/\sqrt{1 + (f/f_c)^2}$, phase $90^\circ - \tan^{-1}(f/f_c)$. A real op-amp's finite gain-bandwidth product eventually turns every active high-pass into a band-pass; the ideal model ignores this.

FIRST-ORDER LOW-PASS, INVERTING

$$H(s) = -\frac{R_f}{R_1} \cdot \frac{1}{1 + sR_fC_f}, \qquad f_c = \frac{1}{2\pi R_fC_f}$$

R_1 from the input to the – terminal, C_f in parallel with R_f in the feedback path, + terminal grounded. Only the feedback pair sets f_c. The passband phase is 180°, so the total phase is $180^\circ - \tan^{-1}(f/f_c)$.

FIRST-ORDER HIGH-PASS, INVERTING

$$H(s) = -\frac{R_f}{R_1} \cdot \frac{sR_1C_1}{1 + sR_1C_1}, \qquad f_c = \frac{1}{2\pi R_1C_1}$$

R_1 and C_1 in series from the input to the – terminal, R_f alone in the feedback path. Only the input pair sets f_c; the high-frequency gain is $-R_f/R_1$.

STANDARD SECOND-ORDER FORMS

$$H_{LP}(s) = \frac{K\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}, \qquad H_{HP}(s) = \frac{Ks^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

$$H_{BP}(s) = \frac{K\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}, \qquad H_N(s) = \frac{K(s^2 + \omega_0^2)}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

K is the passband gain: at DC for the low-pass, at high frequency for the high-pass, at ω_0 for the band-pass, and in both outer bands for the notch. $\zeta = 1/(2Q)$. At $\omega = \omega_0$: $|H_{LP}| = |H_{HP}| = KQ$, $|H_{BP}| = K$ and $H_N = 0$.

SALLEN-KEY LOW-PASS (GENERAL)

$$H(s) = \frac{K}{s^2R_1R_2C_1C_2 + s\left[(R_1 + R_2)C_2 + R_1C_1(1 - K)\right] + 1}, \qquad \omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

C_1 is the capacitor to the output, C_2 the capacitor to ground; DC gain K. Dividing through by $R_1R_2C_1C_2$ gives $Q = \sqrt{R_1R_2C_1C_2}\,/\,[(R_1 + R_2)C_2 + R_1C_1(1 - K)]$.

UNITY-GAIN SALLEN-KEY LOW-PASS (K = 1)

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{(R_1 + R_2)C_2}; \qquad R_1 = R_2 \Rightarrow Q = \frac{1}{2}\sqrt{\frac{C_1}{C_2}}$$

With equal resistors, Q is set by the capacitor ratio alone: Butterworth ($Q = 1/\sqrt{2}$) needs $C_1 = 2C_2$, the feedback capacitor twice the grounded one. Equal R and equal C at unity gain give only $Q = 0.5$.

EQUAL-COMPONENT SALLEN-KEY (LOW-PASS OR HIGH-PASS)

$$R_1 = R_2 = R,\ C_1 = C_2 = C: \qquad \omega_0 = \frac{1}{RC}, \qquad Q = \frac{1}{3-K}, \qquad K = 1 + \frac{R_f}{R_a}$$

Holds for both the low-pass and the high-pass Sallen-Key; the gain alone sets Q. Stable only for $K < 3$: at $K = 3$ the poles reach the $j\omega$ axis and the circuit oscillates at ω_0, and for $K > 3$ they are in the right half-plane. Butterworth: $K = 3 - \sqrt{2} = 1.586$, i.e. $R_f = 0.586 R_a$. At $\omega = \omega_0$ the gain is $KQ = K/(3-K)$.

BUTTERWORTH MAGNITUDE RESPONSE

$$|H(j\omega)| = \frac{K}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^{2n}}}$$

Low-pass of order n (for a high-pass, replace ω/ω_c by ω_c/ω). Maximally flat at $\omega = 0$ (the first $2n-1$ derivatives of $|H|^2$ vanish there), no ripple, exactly −3 dB at ω_c for every n, asymptotic roll-off $20n$ dB/decade, and phase $-n \times 45^\circ$ at ω_c. The poles lie equally spaced on a circle of radius ω_c in the left half-plane. Other standard approximations make different trade-offs: Chebyshev accepts ripple in the passband for a sharper transition at the same order, and Bessel accepts a gentler transition for a nearly constant group delay; all three roll off at $20n$ dB/decade asymptotically.

BUTTERWORTH ORDER REQUIRED

$$n \geq \frac{\log_{10}\left(\dfrac{10^{0.1A_s} - 1}{10^{0.1A_p} - 1}\right)}{2\log_{10}\left(\dfrac{\omega_s}{\omega_p}\right)}$$

A_p = the largest attenuation (dB) allowed at the passband edge ω_p; A_s = the least attenuation (dB) required at the stopband edge ω_s (low-pass: $\omega_s > \omega_p$; high-pass: use ω_p/ω_s). Round n UP to an integer. If ω_p is the −3 dB cut-off, $10^{0.1A_p} - 1 \approx 1$. Example: at least 40 dB at $2\omega_c$ needs $n \geq \log_{10}(9999)/(2\log_{10} 2) = 6.64$, so $n = 7$.

BAND-PASS RELATIONS

$$BW = f_H - f_L, \qquad f_0 = \sqrt{f_L f_H}, \qquad Q = \frac{f_0}{BW}$$

f_L and f_H are the −3 dB frequencies of the overall response. Exact for any second-order band-pass ($f_L f_H = f_0^2$ and $f_H - f_L = f_0/Q$): the centre is the geometric, not the arithmetic, mean of the cut-offs. For a cascade of first-order stages, the stage cut-offs f_1 and f_2 are not the overall f_L and f_H unless $f_2 \gg f_1$ (see above), although the gain always peaks at $\sqrt{f_1 f_2}$.

FIRST-ORDER ALL-PASS (PHASE SHIFTER)

$$H(s) = \frac{1 - sRC}{1 + sRC}, \qquad |H(j\omega)| = 1, \qquad \angle H = -2\tan^{-1}(\omega RC)$$

The input drives both op-amp inputs: through R_1 to the − terminal (with $R_f = R_1$ from the output to the − terminal), and through R to the + terminal, with C from the + terminal to ground. Then $v_+ = v_i/(1 + sRC)$ and $v_o = 2v_+ - v_i$. The gain is 1 at every frequency; the phase goes from 0° at DC through -90° at $\omega = 1/RC$ towards -180°. Swapping R and C gives $H(s) = (sRC - 1)/(1 + sRC)$, phase $180^\circ - 2\tan^{-1}(\omega RC)$.

COMPARATOR (OPEN LOOP)

$$v_o = \begin{cases} +V_{sat}, & v_+ > v_- \\ -V_{sat}, & v_+ < v_- \end{cases}$$

Ideal op-amp, no feedback: the virtual-short rule $v_+ = v_-$ does NOT apply. If the output is limited by a series resistor followed by back-to-back Zener diodes from the limited output node to ground, the levels become $\pm(V_Z + V_D)$ (constant-drop diode model, $V_D \approx 0.7$ V).

DUTY CYCLE OF A COMPARATOR DRIVEN BY A SINE WAVE

$$D = \frac{1}{2} - \frac{1}{\pi}\sin^{-1}\left(\frac{V_R}{V_m}\right)$$

Non-inverting comparator, input $V_m \sin \omega t$, reference V_R with $|V_R| < V_m$; D is the fraction of each period with the output at $+V_{sat}$, and $\sin^{-1}$ is in radians. For the inverting comparator the fraction is $\frac{1}{2} + \frac{1}{\pi}\sin^{-1}(V_R/V_m)$. $V_R = 0$ gives exactly one half.

INVERTING SCHMITT TRIGGER

$$V_{UT} = \frac{R_1 V_{sat} + R_2 V_R}{R_1 + R_2}, \qquad V_{LT} = \frac{-R_1 V_{sat} + R_2 V_R}{R_1 + R_2}$$

$$V_H = V_{UT} - V_{LT} = \frac{2R_1 V_{sat}}{R_1 + R_2}$$

Input to the − terminal; R_1 from the + terminal to the reference V_R (ground if $V_R = 0$), R_2 from the output to the + terminal. By superposition $v_+ = (R_1 v_o + R_2 V_R)/(R_1 + R_2)$ with $v_o = \pm V_{sat}$. With $V_R = 0$: $V_{UT} = +\beta V_{sat}$, $V_{LT} = -\beta V_{sat}$, $\beta = R_1/(R_1 + R_2)$. The output goes LOW when v_{in} rises above V_{UT} and HIGH when it falls below V_{LT}. The loop is centred at $R_2 V_R/(R_1 + R_2)$.

NON-INVERTING SCHMITT TRIGGER

$$V_{UT} = V_R\left(1 + \frac{R_1}{R_2}\right) + \frac{R_1}{R_2}V_{sat}, \qquad V_{LT} = V_R\left(1 + \frac{R_1}{R_2}\right) - \frac{R_1}{R_2}V_{sat}$$

$$V_H = \frac{2R_1 V_{sat}}{R_2}$$

Input through R_1 to the + terminal, R_2 from the output to the + terminal, reference V_R on the − terminal (ground if $V_R = 0$). Switching happens when $v_+ = (R_2 v_{in} + R_1 v_o)/(R_1 + R_2)$ reaches V_R. With $V_R = 0$: $V_{UT} = +(R_1/R_2)V_{sat}$ and $V_{LT} = -(R_1/R_2)V_{sat}$. The output goes HIGH when v_{in} rises above V_{UT} and LOW when it falls below V_{LT}.

RC TIMING (CHARGE OR DISCHARGE TOWARD A TARGET)

$$t = RC\,\ln\left(\frac{V_{final} - V_{initial}}{V_{final} - V_{switch}}\right)$$

Time for a capacitor charging or discharging through R, from $V_{initial}$ toward the asymptote V_{final}, to reach V_{switch} (which must lie between the two). Every period and pulse-width formula in this section and the 555 section is this formula with specific values.

OP-AMP ASTABLE MULTIVIBRATOR

$$T = 2RC\,\ln\left(\frac{1+\beta}{1-\beta}\right), \qquad \beta = \frac{R_1}{R_1 + R_2}$$

An inverting Schmitt trigger (R_1 from the + terminal to ground, R_2 from the output to the + terminal) with R from the output to the − terminal and C from the − terminal to ground. With symmetric $\pm V_{sat}$, each half-period the capacitor charges from $\mp\beta V_{sat}$ toward $\pm V_{sat}$ until it reaches $\pm\beta V_{sat}$, so the output is a square wave with 50% duty cycle and T does not depend on V_{sat}. The capacitor voltage is a chain of exponential segments, not a true triangle. $R_1 = R_2$ gives $T = 2RC\ln 3 = 2.197RC$; $R_1 = 0.86R_2$ gives $T \approx 2RC$.

OP-AMP MONOSTABLE MULTIVIBRATOR

$$T = RC\,\ln\left(\frac{1 + V_D/V_{sat}}{1-\beta}\right) \approx RC\,\ln\left(\frac{1}{1-\beta}\right) \quad (V_D \ll V_{sat})$$

The astable above with a diode across C (anode at the − terminal) that clamps v_C at $+V_D$ (constant-drop model, $V_D \approx 0.7$ V) while $v_o = +V_{sat}$; this stable state needs $\beta V_{sat} > V_D$. A negative trigger pulse at the + terminal sends v_o to $-V_{sat}$; C then charges from $+V_D$ toward $-V_{sat}$, and the circuit flips back when v_C reaches $-\beta V_{sat}$. With $\beta = 0.5$ and V_D neglected, $T = RC\ln 2 = 0.693RC$. After the pulse, C must recover to $+V_D$ before the next trigger.

SQUARE/TRIANGLE GENERATOR

$$V_p = \frac{R_1}{R_2} V_{sat}, \qquad f = \frac{R_2}{4 R_1 R C}$$

Schmitt trigger: R_1 from the triangle output to the + terminal, R_2 from the square output to the + terminal, – terminal grounded. Integrator: input resistor R, feedback capacitor C. The triangle swings between $\pm V_p$ (peak-to-peak $2V_p$; needs $R_1 < R_2$) and the square between $\pm V_{sat}$. From $T/2 = 2V_p/(V_{sat}/RC)$; f is independent of V_{sat} because the ramp rate and the thresholds both scale with it.

555 MONOSTABLE PULSE WIDTH

$$T = RC \, \ln 3 \approx 1.1 \, RC$$

R from V_{CC} to pins 6 and 7, C from there to ground, trigger on pin 2. In the stable state the output is low and C is held discharged. A trigger below $\frac{1}{3}V_{CC}$ sets the output high; C charges from 0 toward V_{CC}, and the pulse ends when $v_C = \frac{2}{3}V_{CC}$. The trigger must return above $\frac{1}{3}V_{CC}$ before T ends (a narrow trigger pulse); in the basic circuit, further triggers during the pulse do not extend it. T does not depend on V_{CC}.

555 ASTABLE

$$t_H = (R_A + R_B) C \ln 2 \approx 0.693 (R_A + R_B) C, \qquad t_L = R_B C \ln 2 \approx 0.693 R_B C$$

$$T = 0.693 (R_A + 2R_B) C, \qquad f = \frac{1.443}{(R_A + 2R_B) C}, \qquad D = \frac{t_H}{T} = \frac{R_A + R_B}{R_A + 2R_B}$$

R_A from V_{CC} to pin 7, R_B from pin 7 to pins 6 and 2, C from pins 6 and 2 to ground. C charges through $R_A + R_B$ and discharges through R_B alone, between $\frac{1}{3}V_{CC}$ and $\frac{2}{3}V_{CC}$ (a ratio of 2 each way, hence $\ln 2$). With D defined as high time over period, D is always above one half and approaches it only when $R_B \gg R_A$. R_A must not be zero, or pin 7 shorts V_{CC} to ground when the discharge transistor turns on.

555 ASTABLE WITH A DIODE ACROSS R_B

$$t_H = 0.693 R_A C, \qquad t_L = 0.693 R_B C, \qquad D = \frac{R_A}{R_A + R_B}$$

A diode across R_B (anode at pin 7) bypasses R_B while C charges, so C charges through R_A only and discharges through R_B only. Ideal-diode result; with a real diode drop, t_H comes out somewhat longer. $R_A = R_B$ gives a 50% duty cycle, and duty cycles below 50% become possible.

555 WITH THE CONTROL-VOLTAGE PIN DRIVEN

$$\text{Astable: } t_H = (R_A + R_B) C \, \ln\left(\frac{V_{CC} - V_{CON}/2}{V_{CC} - V_{CON}}\right), \qquad t_L = R_B C \ln 2$$

$$\text{Monostable: } T = RC \, \ln\left(\frac{V_{CC}}{V_{CC} - V_{CON}}\right)$$

Pin 5 driven to $V_{CON} < V_{CC}$ moves the thresholds to V_{CON} and $V_{CON}/2$. t_L is unaffected (the discharge still halves v_C), while raising V_{CON} lengthens t_H and lowers f. This is how a 555 becomes a voltage-controlled oscillator and, in monostable mode, a pulse-width modulator. $V_{CON} = \frac{2}{3}V_{CC}$ recovers the standard formulas.

VCO CHARACTERISTIC

$$f_o = f_{fr} + K_v v_c \qquad \text{or} \qquad \omega_o = \omega_{fr} + K_o v_c, \quad K_o = 2\pi K_v$$

K_v in Hz/V, K_o in (rad/s)/V. Linear model. Check which unit a question uses before multiplying.

PHASE-DETECTOR CHARACTERISTICS

$$\text{Multiplier: } \bar{v}_d = K_d \sin\theta_e \approx K_d \theta_e \ (\text{small } \theta_e)$$

$$\text{XOR, square inputs: } \bar{v}_d = \frac{V_{DD}}{\pi}\phi, \quad 0 \le \phi \le \pi$$

Multiplier of gain K_m: inputs $V_1 \sin(\omega t + \theta_i)$ and $V_2 \cos(\omega t + \theta_o)$ average to $\frac{K_m V_1 V_2}{2}\sin(\theta_i - \theta_o)$, so $K_d = K_m V_1 V_2/2$ V/rad ($V_1 V_2/2$ for unit multiplier gain). XOR with logic levels 0 and V_{DD}: with 50% duty-cycle square waves a phase difference ϕ apart, the output is high for a fraction ϕ/π of the time, so $K_d = V_{DD}/\pi$ V/rad; $\theta_e = \phi - \pi/2$, measured from the midpoint output $V_{DD}/2$.

LOCKED LOOP: CONTROL VOLTAGE AND STATIC PHASE ERROR

$$v_c = \frac{\omega_i - \omega_{fr}}{K_o}, \qquad \theta_e = \frac{\omega_i - \omega_{fr}}{K_d K_o F(0)} = \frac{\omega_i - \omega_{fr}}{K_V}, \qquad K_V = K_d K_o F(0)$$

Locked loop, linear PD model $\bar{v}_d = K_d \theta_e$, loop-filter DC gain $F(0)$, so $v_c = F(0) K_d \theta_e$. K_V (units 1/s) is the DC loop gain; the 2π cancels if both the offset and the VCO gain are in Hz. A larger K_V gives a smaller phase error for the same offset. With a sinusoidal PD, the second relation gives $\sin\theta_e$ instead of θ_e.

LOCK (HOLD-IN) RANGE

$$\Delta\omega_L = \pm K_o F(0)\, \bar{v}_{d,max}; \qquad \text{multiplier: } \pm K_V, \qquad \text{XOR: } \pm \frac{\pi}{2} K_V$$

$\bar{v}_{d,max}$ is the largest PD output measured from its zero point: K_d for the multiplier (at $\theta_e = \pm\pi/2$), and $K_d\pi/2$ for the XOR, whose characteristic is linear over $|\theta_e| \le \pi/2$. A loop that is already locked stays locked while the input moves up to this far from ω_{fr}, i.e. as far as the largest available control voltage can pull the VCO (assuming the VCO itself can go that far). It depends on the filter's DC gain, not its bandwidth. Some questions quote the total width ($2\Delta f_L$) instead of the one-sided value; read the wording.

CAPTURE (PULL-IN) RANGE, SINGLE-POLE RC LOOP FILTER

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{\tau}} \qquad \Longleftrightarrow \qquad \Delta f_C \approx \frac{1}{2\pi}\sqrt{\frac{2\pi\,\Delta f_L}{\tau}}$$

One-sided ranges; loop filter $F(s) = 1/(1 + s\tau)$ with $F(0) = 1$; an approximation valid when $\Delta\omega_C \tau \gg 1$. Starting unlocked, the PD output is a beat at the difference frequency $\Delta\omega$, which the filter attenuates by about $1/(\Delta\omega\,\tau)$; the loop pulls in only if the attenuated beat still swings the VCO far enough, which gives $\Delta\omega_C \approx \Delta\omega_L/(\Delta\omega_C\tau)$. The capture range never exceeds the lock range. A narrower filter (larger τ) narrows the capture range and leaves the lock range unchanged.

Noise, interference, shielding and grounding

THERMAL NOISE VOLTAGE (THEVENIN MODEL)

$$\overline{v_n^2} = 4kTRB, \qquad V_{n,\text{rms}} = \sqrt{4kTRB}$$

Open-circuit noise of resistance R at absolute temperature T over noise bandwidth B; $k = 1.38 \times 10^{-23}$ J/K. Model: a noiseless R in series with this voltage source. One-sided spectral density $4kTR$ in V^2/Hz.

THERMAL NOISE CURRENT (NORTON MODEL)

$$\overline{i_n^2} = \frac{4kTB}{R} = 4kTGB$$

Short-circuit noise current: a noiseless R in parallel with this current source. Use it for resistors in parallel or for a node driven by a current source.

THERMAL NOISE OF ANY PASSIVE NETWORK (NYQUIST)

$$\overline{v_n^2} = 4kT \int_{f_1}^{f_2} \text{Re}\left[Z(f)\right] df$$

$Z(f)$ = impedance between two terminals of a passive network of resistors, capacitors and inductors, all at temperature T and in thermal equilibrium. Only $\text{Re}[Z]$ contributes. It follows that a network of resistors at one temperature has exactly the noise of its Thevenin resistance.

AVAILABLE NOISE POWER

$$P_n = kTB$$

The maximum noise power a resistor can deliver, into a matched noiseless load $R_L = R$ (load voltage $\sqrt{4kTRB}/2$). It does not depend on R. At $T_0 = 290$ K, kT corresponds to -174 dBm/Hz.

NOISE ON A CAPACITOR (KT/C NOISE)

$$\overline{v_n^2} = \frac{kT}{C}$$

Total mean-square noise across C, integrated over all frequencies, when C is shunted by any resistor R at temperature T: the RC filter's noise bandwidth $1/(4RC)$ cancels R. More generally it follows from equipartition, $\frac{1}{2}C\overline{v_n^2} = \frac{1}{2}kT$, for a capacitor in any passive network in thermal equilibrium. It sets the noise floor of sample-and-hold and switched-capacitor circuits.

SHOT NOISE CURRENT

$$\overline{i_{sh}^2} = 2qI_{DC}B, \qquad I_{sh,\mathrm{rms}} = \sqrt{2qI_{DC}B}$$

$q = 1.6 \times 10^{-19}$ C and I_{DC} = DC current crossing the barrier. In a BJT the base and collector currents carry their own shot noise, $2qI_BB$ and $2qI_CB$. Valid at frequencies well below the reciprocal of the carrier transit time.

FLICKER NOISE IN A BAND

$$S(f) = \frac{K}{f} \;\Rightarrow\; \overline{v_n^2} = \int_{f_L}^{f_H} \frac{K}{f}\,df = K \ln\frac{f_H}{f_L}$$

K in V^2 (or A^2 for current noise). Equal power per decade: each decade adds $K \ln 10 \approx 2.303K$.

WHITE PLUS 1/F NOISE WITH CORNER FREQUENCY

$$S(f) = e_w^2\left(1 + \frac{f_c}{f}\right) \;\Rightarrow\; \overline{v_n^2} = e_w^2\left[(f_H - f_L) + f_c \ln\frac{f_H}{f_L}\right]$$

e_w = white-noise density (for example in $\mathrm{nV}/\sqrt{\mathrm{Hz}}$), f_c = 1/f corner frequency, brick-wall band from f_L to f_H. The same form applies to current noise.

UNCORRELATED SOURCES

$$V_{n,\mathrm{tot}} = \sqrt{V_{n1}^2 + V_{n2}^2 + \cdots + V_{nk}^2}$$

Rms values of independent sources in the same bandwidth. It follows that resistors at the same temperature have, in series, the noise of $R_1 + R_2$ and, in parallel, the noise of $R_1 \parallel R_2$. Series resistors at different temperatures give $\overline{v_n^2} = 4kB(R_1T_1 + R_2T_2)$.

EQUIVALENT NOISE BANDWIDTH

$$B_N = \frac{1}{|H_{\max}|^2}\int_0^\infty |H(f)|^2\,df$$

$H(f)$ = voltage transfer function and $|H_{\max}|$ its peak magnitude (the DC gain, for a low-pass filter). For a white input density e_w, the output noise is $|H_{\max}|\,e_w\sqrt{B_N}$.

FIRST-ORDER (SINGLE RC) LOW-PASS

$$B_N = \frac{\pi}{2}f_{3\mathrm{dB}} = \frac{1}{4RC}, \qquad f_{3\mathrm{dB}} = \frac{1}{2\pi RC}$$

About 1.57 times the 3-dB bandwidth. For an n-th order Butterworth low-pass, $B_N = f_{3\mathrm{dB}}\,\frac{\pi/2n}{\sin(\pi/2n)}$: about $1.11f_{3\mathrm{dB}}$ for $n = 2$, approaching $f_{3\mathrm{dB}}$ as n grows. A single-tuned (parallel RLC) band-pass has the same ratio as the single RC: $B_N = (\pi/2)B_{3\mathrm{dB}}$, with $B_{3\mathrm{dB}} = f_0/Q$.

SIGNAL-TO-NOISE RATIO

$$\mathrm{SNR} = \frac{P_s}{P_n}, \qquad \mathrm{SNR_{dB}} = 10\log_{10}\frac{P_s}{P_n} = 20\log_{10}\frac{V_{s,\mathrm{rms}}}{V_{n,\mathrm{rms}}}$$

The voltage form needs both voltages across the same resistance. Use the rms signal, not the peak.

NOISE FACTOR, NOISE FIGURE AND NOISE TEMPERATURE

$$F = \frac{\mathrm{SNR}_{\mathrm{in}}}{\mathrm{SNR}_{\mathrm{out}}} = 1 + \frac{T_e}{T_0}, \qquad NF = 10 \log_{10} F \ \mathrm{dB}$$

Defined with the source resistance at the standard temperature $T_0 = 290$ K. $F \geq 1$ ($NF \geq 0$ dB), and a noiseless amplifier has $F = 1$. Equivalently, F = total output noise power divided by the output noise power due to the source alone. $T_e = (F - 1)T_0$ is the equivalent input noise temperature. In decibels, $NF = \mathrm{SNR}_{\mathrm{in,dB}} - \mathrm{SNR}_{\mathrm{out,dB}}$.

FRIIS FORMULA FOR CASCADED STAGES

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots$$

Noise factors F_i and available power gains G_i as linear ratios, not dB. When G_1 is large the first stage dominates, so a low-noise, high-gain stage goes first. Same form for noise temperature: $T_e = T_1 + T_2/G_1 + \cdots$

MATCHED LOSSY PASSIVE NETWORK (CABLE, ATTENUATOR)

$$F = 1 + (L - 1)\frac{T}{T_0}, \qquad T_e = (L - 1)T, \qquad F = L \text{ when } T = T_0$$

$L = 1/G \geq 1$ = power loss of the matched two-port as a linear ratio, T = its physical temperature. At T_0 its noise figure in dB equals its loss in dB. Placed before the first amplifier (noise factor F_2), Friis gives $F = L + (F_2 - 1)L = LF_2$: the loss in dB adds directly to the system noise figure.

INPUT-REFERRED NOISE DENSITY WITH SOURCE RESISTANCE R_S

$$e_{ni}^2 = 4kTR_s + e_n^2 + i_n^2 R_s^2 \quad (\mathrm{V}^2/\mathrm{Hz})$$

Multiply by B_N for the mean-square noise and by the gain for the output noise. With low R_s, e_n dominates (a bipolar-input op-amp usually has the lower e_n); with high R_s, $i_n R_s$ dominates (a JFET or CMOS input usually has the lower i_n). Add the feedback resistors' noise separately if it is not negligible.

COMMON-IMPEDANCE COUPLING

$$V_N = I_2 \, Z_c = I_2 \, (R_c + j\omega L_c)$$

I_2 = current of the aggressor circuit in the shared conductor. At high frequency or with fast edges the inductive term $L_c \, dI_2/dt$ usually dominates.

CAPACITIVE COUPLING

$$V_N = \frac{j\omega R C_{12}}{1 + j\omega R (C_{12} + C_{2G})} V_1 \;\approx\; j\omega R C_{12} V_1 \quad \text{for } \omega R (C_{12} + C_{2G}) \ll 1$$

For a low-impedance victim the noise is proportional to ω, R and C_{12}, and leads V_1 by 90°. Equivalent to a current source $I_N = j\omega C_{12} V_1$ from the victim node to ground.

INDUCTIVE COUPLING

$$V_N = j\omega M I_1, \qquad |V_N| = \omega B A \cos\theta$$

M = mutual inductance; B = sinusoidal flux density (an rms B gives an rms V_N), taken as uniform over the loop area A; θ = angle between B and the normal to the loop. Sign: $V_N = -d\Phi/dt$ (Lenz's law); usually only the magnitude matters.

SKIN DEPTH

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

Depth at which a field falls to $1/e$ (37 %) inside a conductor of permeability μ and conductivity σ. For copper: about 9.3 mm at 50 Hz and about 66 μm at 1 MHz.

COMMON-MODE REJECTION

$$V_o = A_d V_d + A_{cm} V_{cm}, \qquad \mathrm{CMRR} = \left| \frac{A_d}{A_{cm}} \right|, \qquad \text{input-referred error} = \frac{V_{cm}}{\mathrm{CMRR}}$$

V_d = differential signal, V_{cm} = common-mode voltage (for example a ground-potential difference). $\mathrm{CMRR}_{\mathrm{dB}} = 20 \log_{10} \mathrm{CMRR}$. An imbalance in source resistances converts part of V_{cm} into a differential error, so the real rejection can be worse than the datasheet CMRR.

SLEW-RATE REQUIREMENT (FULL-POWER BANDWIDTH)

$$\mathrm{SR} \geq 2\pi f_{\max} V_p$$

A sinusoidal op-amp output of peak V_p at frequency $f_{\max}$ is undistorted only if the slew rate meets this; equivalently the full-power bandwidth is $f_{FP} = \mathrm{SR}/(2\pi V_p)$.

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